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# **Science & Technology**

***Japan***

SEMICONDUCTOR INDUSTRY AIMS  
FOR GIGA MEMORIES

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SCIENCE & TECHNOLOGY  
JAPAN

SEMICONDUCTOR INDUSTRY AIMS  
FOR GIGA MEMORIES

906C0053A Tokyo NIKKEI ELECTRONICS in Japanese 22 Jan 90 pp 113-146---FOR  
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### Semiconductor Industry Aiming at Giga Memory Levels

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[Serial articles by Akira Fukuda, Akutaro Kojima, Osamu Kobayashi, Kaoru Fujita, Yoshio Nishimura, and Hidefumi Yokota: "Electronics in the 1990's: Semiconductor Industry Aiming at Giga Level, While Increasing Added Values"]

#### [Text] Introduction

In the 1990's as well, the functions and performance of LSIs will improve at the same pace as before (Figure A).

What will be obtained in the first half of the 1990's include 16M-bit DRAMs, 4M-bit SRAMs, 64M-bit mask ROMs, 100-MIPS microprocessors, and 300,000~1,000,000 gate CMOS gate arrays.

In the latter half of the 1990's, it seems possible to obtain 64M-bit DRAM's, 16M-bit SRAMs, 256M-bit mask ROMs, and 1,000-MIPS (1-GIPS) microprocessors. As for custom LSIs, it will become possible to make automatic designs from specifications.

In the year 2000, sample shipments of 1G DRAMs will begin, and thus we will enter a giga age involving giga bits (G bits) and GIPS.

#### More Importance To Be Given to Profits Than to Shares

However, it will become impossible to achieve "the same rate of progress as that to date" if "the same prices as those to date" are maintained. Semiconductor makers assert that they should "receive more money from semiconductor users" if the same rate of progress is to be attained.

It has become difficult to recover development and manufacturing costs by increasing quantity. Market expansion on a quantitative basis is already slowing down. This has been conspicuous since 1985-1986.

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Figure A. LSIs Expected To Appear in the 1990's

The trends of improvement in integration scale and performance, which were maintained in the 1970's and 1980's, are likely to be maintained in the 1990's as well.

		1990	1993	1996	1999
Memory LSI	DRAM	4M~256K bit	16M~256K bit	64M~1M bit	256M~1M bit
	DRAMs in largest mass sale	1M bit	4M bit	4M~16M bit	16M~64M bit
	SRAM	1M~16K bit	4M~64K bit	16M~256K bit	64M~256K bit
	Mask ROM (with largest capacity only)	16M bit	64M bit	256M bit	1G bit
Micro-processor	Performance Architecture 1-chip micro-computer	100 MIPS 32 bit 16 bit		1,000 MIPS (1 GIPS) 32 bit (64 bit?) 32 bit	
Custom LSI	LSI chip  Design system  Form of expression	CMOS channelless gate array with 300,000~1,000,000 gates Logical synthesis, module generator Functional description		Standard cell of CMOS building-block type  Silicon compilation  Operational description	
LSI manufacturer technique	Minimum processing size Process	0.8 $\mu$ m  CMOS	0.6 $\mu$ m  CMOS	0.4 $\mu$ m  CMOS (bipolar CMOS)	0.3 $\mu$ m  CMOS (bipolar CMOS)

The prices of DRAMs that represent memory LSIs were generally constant from the early 1970's to the early 1980's. During this period, the DRAM capacity increased at the rate of four times every 3 years. In spite of this, the DRAM quantity increased as rapidly as 10-fold in 10 years. Thus, the high rate of increase in quantity made DRAM prices constant.

However, this increase has been slowing down since the memory depression in 1985, with this as a turning point. Before 1985, the total bit demand approximately doubled annually, but this slowed down to an increase of 1.5~1.6 times. Many semiconductor makers take the view that the growth rate will develop at this rate in the 1990's as well.

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If the DRAM capacity expands at the same rate as previously (four-fold every 3 years), with the annual increase in total bit demand remaining 1.6-fold, the quantity of DRAMs will decrease slightly (Figure B). To recover the investments in technological development and manufacturing facilities, there is no other way but to raise DRAM prices.

The rise in price is not limited to DRAMs. There is the possibility that this will extend to all LSIs to be manufactured using the same fine patterning technology in the same duration. However, per bit and per gate prices will continue to drop, with the speed of the drop slowing down.

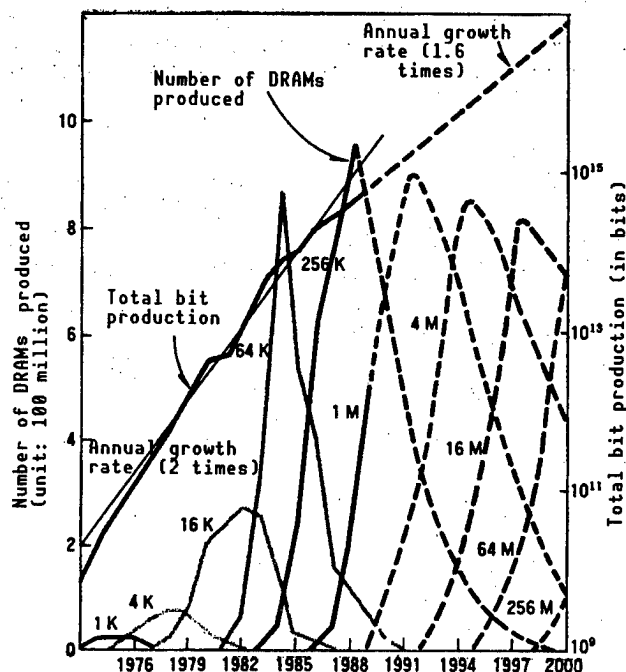


Figure B. Total Bit Demand and DRAM Production

During 1985-1986, the annual growth rate of total bit demand fell from 2 times to 1.6 times. The increase in DRAM production will stop and it will decrease gradually.

### User-Maker Affiliation, Specialization, and Tie-Ups Will Progress

The semiconductor industry has reached a stage of covering cost by added values. Many makers and users predict that the annual average growth rate in the 1990's will be 10-15 percent in both the domestic and overseas markets. Semiconductor makers say that this growth will be achieved just through higher LSI prices.

Various added values for LSIs are expected in the 1990's, such as functions, performance (speed), and integration.

To make the function of LSIs such an added value, semiconductor makers want to conceive new functions and to market LSIs equipped with these functions (ASSP).

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However, the most advanced functions are created by makers of the most advanced electronic machinery and equipment. These functions go over to semiconductor makers through custom LSIs. Thus, the ties between specific users and makers gather strength (Figure C), and they are affiliated with each other.

Users (set makers) sought by semiconductor makers
<ul style="list-style-type: none"><li>▷ Rich in WHAT (seeds of general-purpose LSIs)</li><li>▷ Able to master silicon compilation</li><li>▷ Issue orders for large quantities of custom ICs</li><li>▷ Consume large amounts of memories</li></ul>



Semiconductor makers sought by users (set makers)
<ul style="list-style-type: none"><li>▷ Equipped with microprocessing technology</li><li>▷ Have silicon compilation</li><li>▷ Rich in package articles</li><li>▷ Have many support personnel</li><li>▷ TAT is short</li><li>▷ Unit price of chips is low</li></ul>

Figure C. Semiconductor Makers Sought by Semiconductor Users, and Semiconductor Users Sought by Semiconductor Makers

In the latter half of the 1990's, it will become possible to make automatic designs for custom LSIs. However, it is likely that only a limited number of semiconductor users and makers will gain access to this field.

The quick way to make the speed and integration of LSIs their added values is to take the lead in microprocessing technology. Many Japanese semiconductor makers pursue added values at this point. However, they need large investments

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for this purpose, and the number of semiconductor makers that can continue such investments is limited.

Moreover, it has become possible to invest in all technologies and manufactured products since the semiconductor industry has become so broad. Therefore, it is desirable to narrow the technologies and manufactured products to some extent. With specialization making progress, what is insufficient should be made up through tie-ups.

In the case of multipurpose articles, specialization by semiconductor makers will bring a decrease in the number of makers per item. In the eyes of users, this is an oligopolistic development.

### Part 1. Semiconductor Industry Is Also Shifting Emphasis From Quantity to Quality

Improvement in the function and performance of LSIs will continue in the 1990's as well. In the year 2000, 1G-bit DRAMs and 1,000-MIPS (1-GIPS) microprocessors will appear in the market. Custom LSIs can be designed to match user's descriptions of functions they desire. The possibility of realizing these is not insignificant. However, it is likely that the number of makers capable of producing such advanced LSIs and that of users capable of obtaining them will be limited. The prices will rise to a fairly large extent. LSI makers' tendency to choose LSI users will become strong. LSI makers will promote specialization and sharing.

LSIs will continue to make progress in the 1990's too, at the same tempo as before. They are likely to improve for the next 10 years with the same trend. In the year 2000, users will be able to obtain sample 1G DRAMs and 1-GIPS (1,000-MIPS) microprocessors. Thus, a "giga age" will be reached. It will become possible to produce custom LSIs if users just input their specifications. This means an automatic design.

However, it is not likely that many users will actually be capable of buying these LSIs, because the prices of 1G DRAMs and 1-GIPS microprocessors will very likely rise far higher than current prices.

The reasons for this will be given in detail later on. Here we will just look over the predictable progress of LSIs in the 1990's (Table 1).

#### First Half of the 1990's: Integration and Capacity Will Improve Smoothly

In the first half of the 1990's, the integration scale and performance of LSIs will be improved comparatively smoothly.

The capacity of memory LSIs will expand fourfold every 3 years, as has been the case to date. Recently, general-purpose 4M DRAMs have appeared in large numbers, and mass production of 16M DRAMs will begin. In the case of DRAMs, too, the lifespan of low-capacity products will become longer than ever, and 64Kx4-bit DRAMs will still be obtainable. The number of memories for exclusive use will be on the increase, focused on images.

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Table 1. Progress of main LSIs in the 1990's

		1990	1993	1996	1999
Memory LSI	DRAM	4M~256K bit	16M~256K bit	64M~1M bit	256M~1M bit
	DRAMs in largest mass sale	1M bit	4M bit	4M~16M bit	16M~64M bit
	SRAM	1M~16K bit	4M~64K bit	16M~256K bit	64M~256K bit
	Mask ROM (with largest capacity only)	16M bit	64M bit	256M bit	1G bit
Micro-processor	Performance Architecture 1-chip micro-computer	100 MIPS 32 bit 16 bit		1,000 MIPS (1 GIPS) 32 bit (64 bit?) 32 bit	
Custom LSI	LSI chip  Design system  Form of expression	CMOS channelless gate array with 300,000~1,000,000 gates Logical synthesis, module generator Functional description		Standard cell of CMOS building-block type  Silicon compilation  Operational description	
LSI manufacturer technique	Minimum processing size Process	0.8 $\mu$ m  CMOS	0.6 $\mu$ m  CMOS	0.4 $\mu$ m  CMOS (bipolar CMOS)	0.3 $\mu$ m  CMOS (bipolar CMOS)

As for microprocessors, the performance of 32-bit general-purpose processors will exceed 100 MIPS, and thus they will come to have the same performance as mainframes of the highest class (general-purpose supercomputers).

Among 16-bit microprocessors, one-chip microcomputers will be in common use. Chips for exclusive use and custom chips will flood the market.

In the case of custom LSIs, users will be able to design LSIs through functional descriptions, supported by design techniques including logical synthesis and module generators. As for LSI chips, a CMOS channelless gate array with 300,000~1,000,000 gates (load scale of LSI makers) will constitute the mainstream.

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### Latter Half of the 1990's: Waves of Exclusive Use and Customization Will Mount

With the advent of the latter half of the 1990's, the pace of improvement in integration and performance will become sluggish, because the hurdle to manufacturing technology is expected to become higher. Here we will give explanations on the assumption that this hurdle has been overcome.

Among general-purpose DRAMs, 16M-64M bit products will be manufactured most plentifully, but mass production of 256M-bit DRAMs will begin. Around that time, 1M (256K x 4-bit) products will be machines having the smallest capacity from 1M to 256M.

The trend toward putting memory LSIs to exclusive use will continue further, and custom memories will be widely used for HDTV, etc.

The performance of microprocessors, if improved in the same way as in the first half of the 1990's, will reach 1,000 MIPS. However, the architecture following that on the 1,000 MIPS level is not as yet visible. There is also the possibility that 64-bit microprocessors will appear.

The trends of 32-bit microprocessors will focus on their being put to exclusive use and on customization. The current digital systems will mostly come to stay in one chip.

As for custom LSIs, users will become able to make designs from the specifications they desire. Only operational descriptions will suffice for them, for they are to be supported by silicon compilations. LSI chips will serve as CMOS standard cells of building-block type.

The waves of exclusive use and customization will cover most LSIs. "The latter half of the 1990's will be an age of ASSP, with functions and specifications realized by large-scale circuits, integrated in one chip, won't it?" (Hitachi executive director and electronic business group manager Kazuo Kanehara). For the distinction of electronic machinery and equipment, "portions that can be customized will be necessary" (Fujitsu electronic device business group manager Junichi Mogi).

### Increase in Investment Will Push Up Prices

If the LSIs for the future can be obtained at the same prices as those available today, users will be very happy. But this is very unlikely, as mentioned earlier. The prices of LSI chips are going to be higher in the future.

However, the unit price per integrated device will show a continued downward trend. The per-bit price of memory LSIs and per-gate price of gate arrays will drop in the 1990's as well. What is different from the 1980's is that the drop in price will slow down.

The direct reason for this is that microprocessing will gradually become difficult (as explained in detail in Part 6), and that, therefore, development and manufacturing will become very high, according to semiconductor makers.

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Even judging from the trend of facilities investments to date, for example, the costs will run up to huge amounts.

It is even estimated that ¥1 trillion must be invested in creating a pre-process (wafer process) line to produce 10 million 64M-bit DRAMs per month (according to a former director of a certain major semiconductor manufacturing company). This is the most optimistic estimate, assuming no technical obstacles.

Investments in semiconductor facilities depreciate at a rate of 50 percent in the first year, 40 percent the second year, and 10 percent the third year, for example, and thus the depreciation must be completed in 3 years (according to a semiconductor maker). When an investment amounts to ¥1 trillion, it must be depreciated by half—about ¥500 billion—in 1 year. Since 120 million DRAMs are produced annually, it will be impossible to absorb the depreciation unless they are sold for more than ¥5,000 each.

Because of the increase in the burden of investments, the "bi-rule" (meaning that the per-chip bottom price rises twofold each time one generation is followed by the next generation<sup>6</sup>), advocated in 1987, is being recognized among semiconductor makers.

When a DRAM price is extrapolated from a 256K-bit DRAM in accordance with the bi-rule, a 256K product will be priced at ¥300~350, a 1M product at ¥600~700, a 4M product at ¥1,200~1,400, a 16M product at ¥2,400~2,800, and a 64M product at ¥4,800~5,600. This generally agrees with the "¥5,000 or more," mentioned above.

### Prices Tend To Depend on Microprocessing Techniques

DRAMs are not the only products that urge semiconductor makers to appeal for price rises. Such products include not only memory LSIs but also all other LSIs manufactured by microprocessing techniques of the same degree. "Prices of logic circuits and processors will also rise," says NEC director Gen Sasaki.

The first-generation 4M DRAMs, for example, are generally manufactured by the CMOS technique with the smallest processing size of 0.8  $\mu\text{m}$ . The 1M DRAMs in the preceding generation are manufactured with a 1.2  $\mu\text{m}$  CMOS size. If the price of a 4M DRAM is twice that of a 1M DRAM, users will be expected to accept the same case for both the 1.2  $\mu\text{m}$  and 0.8  $\mu\text{m}$  gate CMOS gate arrays.

Some may say, "How ridiculous it is to go to the point of raising the price of gate arrays, even apart from the price of memories!" Certainly, gate arrays have been cheap so far, but this is because old lines depreciated by memory LSIs have been used. When memory LSIs were manufactured with the 1.2  $\mu\text{m}$  line, there were many cases where gate arrays and one-chip microcomputers were manufactured with the 2.0  $\mu\text{m}$  line. This inevitably caused their prices to fall.

Furthermore, competition among the makers of gate arrays continued to lower prices, and users became accustomed to the low price. They even expected that silicon would become free.

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However, beginning with the LSIs of an 0.8  $\mu\text{m}$  rule, mass production of memory LSIs and CMOS gate arrays will begin almost simultaneously.<sup>7</sup> We hope that gate arrays also will help in the depreciation of manufacturing facilities. Compared with memory LSIs, it is difficult to reduce the price of gate arrays alone.

### End of "Infancy"

Semiconductor makers attribute the increase in cost to the price rise. For more than 10 years, however, the expansion of facilities investments has been a problem.<sup>3</sup> Why have semiconductor makers unanimously begun to disapprove the price development up to the present?

Basically, this is largely due to the slowdown of the quantitative growth of the semiconductor market. So far, the increase in the cost for development and for investments has been covered by the increase in the quantity of production. It has been possible to create sufficient demand so that costs are reduced through mass production. In the future, however, it will become impossible to expect a sufficient increase in quantity to compensate for the investment cost.

### Efforts To Be Made With the Electronics Industry for Structural Change

From the 1970's to the 1980's, the semiconductor industry rapidly expanded its scale together with the electronics industry. The cost reduction and quantitative expansion caused the market to expand. Since 1985, this development cycle has been collapsing. The semiconductor industry is undergoing a structural change.<sup>2</sup>

As a result, trends in the 1990's will progress toward 1) giving importance to added values (rise in LSI prices); 2) screening or product series (specialization and oligopoly) and sharing; 3) tie-ups between makers (mutual complementarity); and 4) tie-ups (affiliation) between makers and users.

The fundamental reason for these trends is that the growth of the semiconductor industry has slowed down. The scale of this industry, which expanded as a result of rapid growth, has ceased to allow such growth to continue. It has fallen into a state where "a big ball rolls slowly" (NEC director Sasaki).

### The Growth of the Market Will Slow Down

The growth rate of the semiconductor market has been slowing down since the depression of 1985 (Figure 1).

There has been exceptionally high growth in domestic semiconductor production in terms of yen value. The average growth rate in 1975-1980 was 26 percent and in 1980-1985, 23 percent.

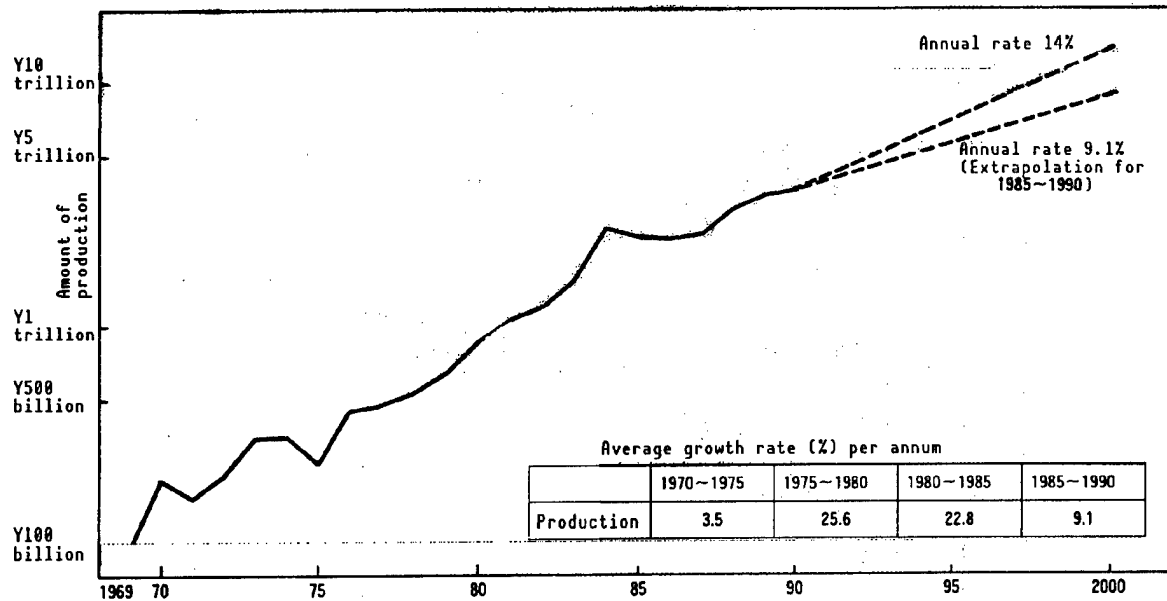


Figure 1. Development of Domestic Production of Semiconductors (1969-1990)

A slowdown is seen in the growth rate from 1985. The value in 1989 is partly estimated and that in 1990 is entirely estimated by this magazine. (Data: machinery statistics by MITI (Ministry of International Trade and Industry))

In contrast, the growth rate in 1985-1990 is likely to be limited to an annual average of 9 percent (predicted by this magazine). According to a forecast by WSTS (World Semiconductor Trade Statistics), the annual average growth rate of domestic demand for semiconductors in 1988-1992 will be 8.2 percent (Figure 2). Both forecasts indicate that the growth rate will be lower than that before 1985.

The growth rate in the 1990's will also be lower than that before 1985. A midterm view compiled by MITI estimates that the annual average growth rate of domestic demand for semiconductors in 1987-2000 will be 13.6 percent.<sup>5</sup> The annual average growth rate of production in the 1990's, mentioned in interviews with Japanese semiconductor makers, was also estimated to be 10-15 percent. According to all these forecasts, the growth rate will not return to 20 percent or higher.

This growth rate itself is exceptionally high as compared with other industries. First, the electronics industry is regarded as showing a comparatively high growth rate—close to 10 percent.<sup>8</sup> In addition, the rise in the rate of semiconductors included in electronic machinery and equipment, as well as the fundamental nature (Figure 3) of semiconductors to the effect that "they cause other industries to become oriented toward electronics,"<sup>4</sup> guarantees a growth rate higher than that in the electronics industry. "We have decided to gain access to LSI business because the growth rate of the market is high. Friction will arise in a world showing no growth," says Koichi Igarashi, manager of the LSI business promotion division, new business group of Kawasaki Steel Corp.

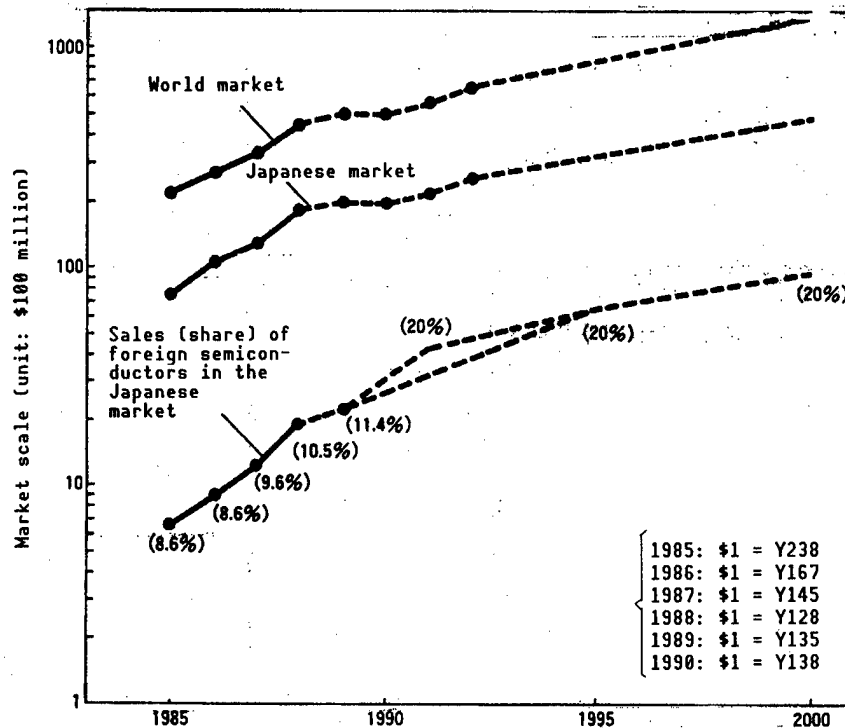


Figure 2. Demand for Semiconductors in the World and in Japan (1985-1992), and the Sales of Foreign Semiconductors in Japan

The sales of foreign semiconductors in Japan in 1989 are forecast by this magazine. The extrapolated values in 1995 and 2000 are based on the assumption that the shares are estimated at 20 percent. The semiconductor demand in 1989-1992 is predicted by WSTS. The demand in 1993 and thereafter is based on the values extrapolated by this magazine. (The data were obtained from WSTS, MITI, and the Japan Society of Electronic Machine Industry.)

The problem is that the growth is slower than in the past. This will make it impossible to use the expansion cycle of the market to date or to expect a quantitative expansion through cost reduction. Thus we will be urged to convert to the policy of attaching importance to added values.

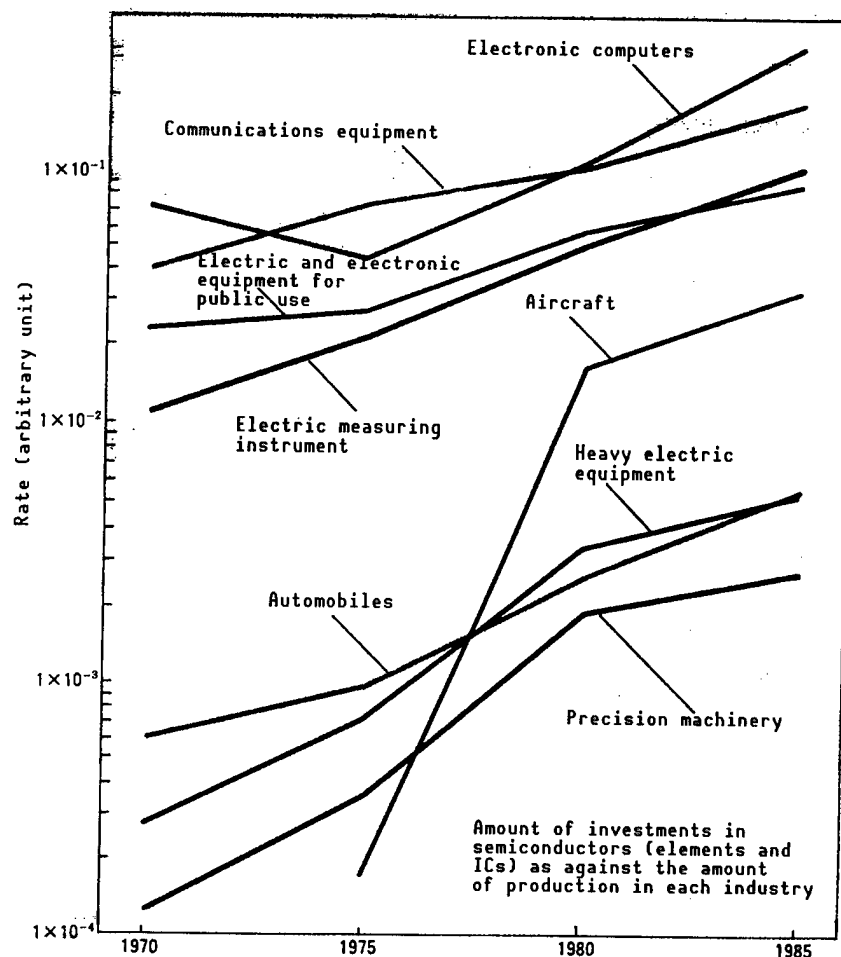


Figure 3. Changes in Ratio of Semiconductors to the Amounts of Production in Various Industries (1970-1985)

This illustration shows the cost of semiconductors as a proportion of total production costs in each industry. The figure 0.3, for example, shows that ¥3,000 worth of semiconductors were spent in manufacturing a product worth ¥10,000. It can also be said to indicate the rate of electronization in each industry.

(Note: The classification of industries is based on industry-related tables. The numerical figures obtained by the Industrial Bank of Japan on the basis of industry-related tables were graphed by NIKKEI ELECTRONICS.)

#### Use of One Chip for Electronic Equipment Will Also Urge Conversion

LSIs have been making progress through the expansion of integration scale. This also will bring about the change to the trend toward attaching importance to added values<sup>1</sup> (Figure 4).

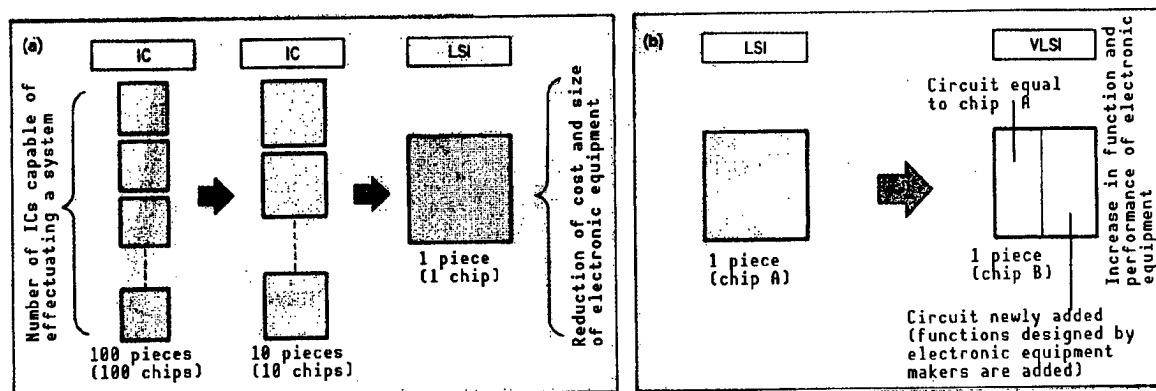


Figure 4. Structural Change Before and After Using One Chip for Electronic Equipment (Change in effects exerted by the improvement of IC integration upon electronic equipment)

(a) The age when electronic equipment was produced with many IC chips: In the age when electronic equipment consisted of 100 ICs, the improvement in the degree of IC integration directly led to reducing cost and size. In the 1970's, when it became possible for electronic equipment consisting of 100 ICs to be operated with 10 ICs, the IC cost and the packaging area became about one-tenth of what they had been. The improvement in the degree of integration resulted in an increase in the value of electronic equipment (cost reduction). Thus the sales of electronic equipment increased at a rate exceeding that of the cost reduction. The amount of IC production also increased, and this promoted the expansion of the market.

(b) The age when electronic equipment can be operated with one chip: The situation has changed since it became possible to operate electronic equipment with one chip. The price of the equipment has fallen so far that increased sales do not follow even additional cost reductions. The integration of LSIs increased further to produce VLSIs, in which the LSI circuit occupies only half the area of the chip. Use of the remaining half will enable production of multifunctional equipment with improved performance. This is a point to be noted by electronic equipment makers. It has become impossible for the improvement in integration to be "directly" linked with an increase in the value of equipment.

It is not that this change will occur rapidly with the use of one chip for a system as a turning point. It will take place gradually with a decrease in the number of ICs that constitute a system.

The development of the electronics industry from the 1970's to the 1980's was the result of the reduced cost and the mass production of electronic machinery and equipment. The cost reduction was supported by the expansion of the scale of IC integration.

Suppose that it has become possible for electronic equipment, first composed of a 100-chip IC, to be formed with a 10-chip LSI because of an expanded scale of IC integration. If electronic equipment sells in this case in quantities large enough to absorb the cost of LSI development and production facilities, the unit price of LSIs will not have to be raised very markedly, and it will

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be possible to reduce the cost of electronic equipment. This is equivalent to the case of reducing the price of a color TV set, for example, that was worth nearly ¥300,000, and thereby improving the sales.

Through expanding the scale of IC integration and reducing the cost, electronic equipment makers sold their products in great quantities that largely covered the fall in price due to cost reduction. Thus, both the makers and users profited.

However, the cost reduction for electronic machinery and equipment will become meaningless some day; products will cease to sell even if the cost is reduced. Even if the price of a color TV set is reduced from ¥30,000 to ¥20,000, for example, the sales will not increase. This will make it difficult to recover investments even if a new LSI is developed. Thus, a change in thinking about both electronic equipment and semiconductors, will be inevitable. Cost reduction will not be effective any longer, and importance will come to be attached to added values.

Suppose that it were possible at this time to fabricate electronic equipment with a one-chip LSI. This too would promote the idea of giving importance to added values.

Since the expansion of integration scale is continuing, an LSI still larger in scale (VLSI) will appear in the near future. If this VLSI is used, it will become possible to store the basic circuit of electronic equipment in one part of a chip.

Both an LSI and a VLSI have one chip each. Now this can hardly contribute to cost reduction; therefore, makers of electronic machinery and equipment move toward attaching importance to added values. They shift to VLSIs and, storing the surplus space of a chip with the functions, specifications, etc., that they have designed, they try to sell their new products at high prices with these added values. It is desirable for the price of this VLSI to be the same as that of an LSI, because it is the electronic equipment makers themselves who have designed the added values.

However, semiconductor makers have begun to say that they do not want the price of the VLSI to be the same as that of the preceding LSI. But even when VLSIs are sold at the same price, the quantity of sales hardly increase, making it difficult to recover the investments in development and facilities.

It is certainly possible for semiconductor users to avoid expensive VLSIs. It is not necessary to choose one chip against one's will. A trend will grow toward a "multichip" structure for the basic circuit and added functions to remain divided in separate LSIs. On the other hand, semiconductor users truly wanting the one-chip system will buy VLSIs even when they are expensive.

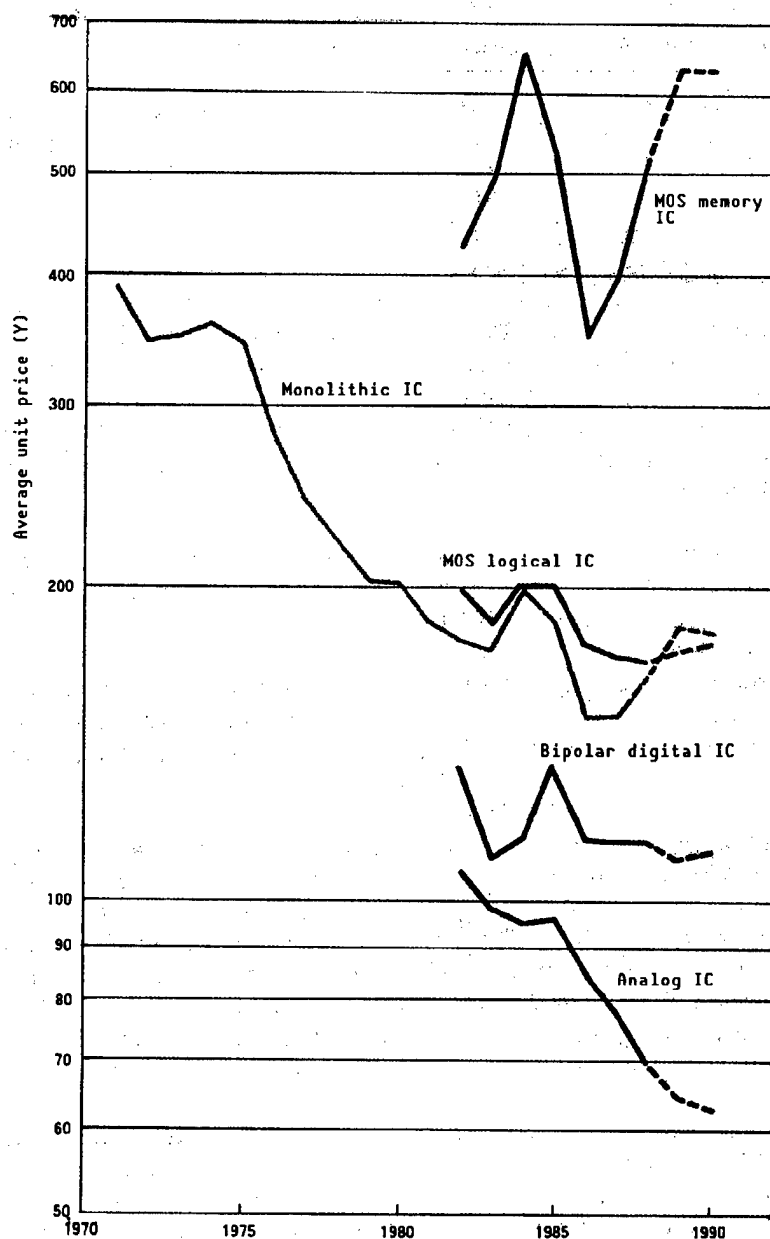


Figure 5. Change in the Average Unit Price of ICs (1971-1990)

In the 1970's, the average unit price of monolithic ICs continued to fall. the unit price dropped from about ¥390 (1971) to about ¥200 (1980).

However, it stopped falling when the 1980's began. There is the strong fear that the price may reverse in the 1990's. The values in 1989 were partly estimated by NIKKEI ELECTRONICS, and those in 1990 were totally estimated by the same magazine company. (Data: MITI's annual report on machinery statistics.)

### Unit Price of ICs Will Rise After Dropping

From the 1970's to the 1980's, the average unit price of integrated circuits (monolithic ICs) continued to fall (Figure 5). On the other hand, the cost of monolithic IC production increased rapidly. In this period, the rapid increase in quantity absorbed the cost for ICs and thus expanded the market (monetary amount).

With the arrival of the 1980's, the unit price tended to stop falling. This can be taken to mean that the quantitative expansion has gradually become unable to absorb the cost. Thus, the unit price is currently going to shift to an upward trend.

### Where Should Added Values Be Attached?

Semiconductor makers want to sell LSIs at a high price. The LSI is basically an industrial product of mass production type. It is desirable to obtain an added value while making the most of this characteristic.

Is the added value the function of the LSI, its performance, or the scale of its integration?

One kind of LSI is an ASSP, a marketed article with a function (feature) regarded as an added value.

For this purpose, custom LSI business is important. Semiconductor makers want to develop an LSI loaded with new machinery specifications (equivalent to WHAT) jointly with the foremost electronic apparatus makers. The semiconductor makers on their part want to sell these LSIs to second-level and lower-level electronic equipment makers in terms of ASSPs.

Therefore, LSI makers want to strengthen their ties with electronic equipment makers who can bring forth many equipment specifications (WHAT) that are likely to be adopted for ASSPs. Thus, the ties between semiconductor makers and semiconductor users are strengthened, and this brings about a move toward affiliation.

Among the items that U.S. semiconductor makers have been strongly demanding of Japanese semiconductor users since the beginning of the Japan-U.S. semiconductor trade friction is a "design in" (joint development of LSIs between electronic apparatus makers and semiconductor makers at the stage of apparatus development). It can be said that such an item is also designed to obtain apparatus specifications (WHAT). U.S. semiconductor makers include many who are exclusively engaged in the manufacture of semiconductors. Unlike Japanese semiconductor manufacturers having electronic apparatus divisions within themselves, they can hardly introduce new apparatus specifications into semiconductors.

### Japanese Makers Are Striving Hard With Manufacturing Techniques

Many Japanese semiconductor makers take advantage of the performance and integration scale of their products. They seek to increase the speed of their LSIs and to expand their integration scale by making free use of the most advanced manufacturing techniques. They want to have semiconductor users recognize these as added values.

In the case of logical LSIs, the operational speed and the number of gates are equivalent to these features and in the case of memory LSIs, access time and memory capacity are equivalent to them. These are determined to some extent on the basis of microprocessing technology.

Japanese semiconductor makers are strong in manufacturing technique in comparison with design technique. They can reduce the processing size from 0.8  $\mu\text{m}$  to 0.5  $\mu\text{m}$ , or further to 0.3  $\mu\text{m}$ . They do not relax their efforts in the development of microprocessing technology. For this purpose, huge investments for development and production facilities are required. Not many semiconductor makers can continue to make such investments. Moreover, the costs increase as the processing technique becomes microscopic, and this pushes LSI prices up further.

### Competition Among Semiconductor Makers Will Be Avoided

You may say that the prices have been the same even since the increase in function, performance, and capacity.

There are cases of prices not being raised or being reduced even when the recovery of investment cost cannot be expected. These cases arise in times of excessive competition and also of struggles for shares. Makers turn to low-price competition and struggle for shares. Users, however, can obtain cheap semiconductors.

But such excessive competition has become difficult for two reasons:

1) semiconductor makers are strengthening their specialization, and 2) they are deepening their ties with semiconductor users. Such trends have become conspicuous since the depression of 1985.

"Three-generation DRAMs should be developed simultaneously, but the number of semiconductor makers capable of such development will be limited" (Toshiba director Go Kawanishi). "We want our development to be focused on ASICs" (Junichi Mogi, deputy manager of the Fujitsu electronic device business group). "As for mask ROMs, we will firmly maintain our top level in the 1990's as well" (Hiroshi Inoue, Sharp director and manager of the IC business group).

It is since 1985 that semiconductor makers have been rapidly strengthening their specialization. Herein lies their conversion from an "all-purpose" type of production to a priority principle, with their own advantages emphasized.

Their shift to specialization is designed also to avoid dispersion or development investments and resources. To disperse risks, it is better to have many product series; however, now that the semiconductor industry has become so large in scale, such a large variety of products cannot be dealt with by a single enterprise. "Even in increasing the series of manufactured products, we will specialize our products to some extent," says Takashi Kitaoka, Mitsubishi Electric Corp. executive director and manager of the electronic device business group.

#### **Specialization, Sharing, and Oligopoly**

Semiconductor makers will promote sharing also at the same time as specialization. This will also lead to a move to avoid excessive competition, and will strengthen the sharing of roles classified by manufactured products and by techniques.

In the eyes of semiconductor users, this is evidently a trend toward oligopoly. More accurately, it is probably a trend toward oligopoly along product lines.

The production of general-purpose, 32-bit CISC processors is virtually controlled by Intel and Motorola of the United States. On the other hand, however, sharing of the market is under way, with Japanese semiconductor makers handling 4-8-bit one-chip microcomputers.

The same is the case with memory LSIs. Sharing is taking place by the kind of products in terms of DRAMs, SRAMs, EPROMs, and mask ROMs, as well as by memory capacity in terms of large-capacity and small-capacity products.

As a result, the current leading products, including DRAMs, will be manufactured for a longer time than previously. So far, small-capacity products have disappeared with the appearance of large-capacity products. In the future, such products will disappear gradually after remaining on the market for a long time.

Nonvolatile memories are already in a state where small-capacity products will remain, without disappearing. SRAMs are also moving toward such a state. This shows that the number of serviceable electronic apparatuses is increasing when a memory LSI has several chips at most. The rise in the price of large-capacity products will bolster this trend. In the case of DRAMs, too, several generations of products will overlap one another in the 1990's, as in the case of other memory LSIs.

#### **Tie-Ups Will Increase Further**

If specialization makes too much progress, it will become impossible to arrange products as an LSI kit that constitutes electronic equipment. Therefore, the OEM among semiconductor makers will become more active than ever. This is already active at present.

Tie-ups except for OEM will also increase more and more, including those for the development of technology, for example. It has become difficult for a single semiconductor maker to develop multiple technologies. Therefore, new products are being jointly developed, with one semiconductor maker emphasizing his switching times and another maker contributing complementary techniques. Or a semiconductor maker is allowed to use the intellectual property right (CPU core, for example) of his cooperating partner in exchange for furnishing his manufacturing technique. Such international tie-ups are active.

For such complementary practices to materialize, the advantage and disadvantage of one's company must be distinct. Makers moderately strong in everything (but not on the top level) are not suitable for tie-ups.

#### **Affiliation Between Users and Makers**

The number of tie-ups between semiconductor users and makers is also likely to increase. Since the depression of the 1980's, such moves have been conspicuous in the case of DRAMs. Semiconductor users want to ensure a long-term stable supply of DRAMs, even if this costs them some money. Semiconductor makers want to have customers who will purchase their products in certain quantities regardless of market fluctuation.

This is exemplified by the DRAM manufacturing company jointly set up by Acer, a computer maker of Taiwan, and Texas Instruments of the United States. In this joint venture, Texas Instruments is obligated to supply DRAMs it has manufactured to Acer at a certain rate.

#### **Competition Will Become Partial**

Even if specialization, sharing, or tie-ups make progress, the fierce competition will not necessarily cease altogether. However, it is less likely that competition will involve all kinds of semiconductors; the competition will become partial.

In the latter half of the 1980's, RISC processors surfaced rapidly. Competition in this field is fierce because the market itself, created through a combination of RISC processors and workstations, is on its way to rapid growth starting from zero.

Even so, the growth of the RISC processor market will not exert much influence on the growth of the entire semiconductor market.

DRAMs are likely to suffer the most from excessive competition: many fear that 4M-bit DRAMs may bring about price-lowering competition.

Price competition may occur and enable users to obtain cheap DRAMs temporarily. Through such competition, however, DRAM makers will undergo another screening. If so, the number of makers on the 4M level will decrease and their DRAM-supplying capacity will drop. In the 16M field, there is the strong fear that prices will rise, with a shortage of DRAMs coupled with oligopoly.

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Specialization, oligopoly, and affiliation are fundamentally related, another indication that the industry is moving toward maturity.

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Part 2. The 1990's as Viewed by Top-Level Semiconductor Makers

We had top-level leaders of major Japanese semiconductor manufacturing companies state their views of the semiconductor industry in the 1990's and the policies of the various companies. Many makers are largely changing their business policies from the all-purpose type of "handling everything" to a priority principle to "improve some strong points" they have. They say that they must have individuality for the very purpose of achieving international cooperation.

General Sasaki, NEC, director and manager of semiconductor business group: "We will make steady investments while avoiding diffusion of power."

"After the depression of 1985-86, we realized that demand does not expand infinitely. At that time, it was expected that demand for 256K-bit DRAMs would expand because of the drop in price. However, that proved to be an illusion. Consumption of memories increased along a certain trend, but there was no great change after the price drop.

"Flood-like investments are not good; steady investments are better. If the current progress in technology continues, we will form the newest and the most efficient manufacturing line every year, one by one. We will continue this undertaking for the coming 3 or 4 years. NEC can make investments amounting to ¥100 billion or so every year. It can form at least one diffusion line. We will not increase the number of our production bases in the United States or in Europe, but will just reinforce them, for the time being. We want to avoid the diffusion of resources.

"In the 1990's, manufacturers products and technologies will become diverse. We need manpower for each technology, but it is difficult to procure manpower for all technologies. So it is necessary to complement it mutually for the respective technologies. NEC's strong points cannot be generalized. In cooperating with MIPS Computer Systems of the United States, NEC had strong points in semiconductor technology and productivity and in its being a leading company dealing with microcomputers."

Go Kawanishi, Toshiba, managing director: "Waves of silicon cycles will become small."

"With an eye on the 1990's, Toshiba is carrying out 1) constant, large-scale investments; 2) constant technological investments; 3) simultaneous development of three-generation DRAMs (4M-, 16M-, and 64M-bit DRAMs); and 4) systematization (joint development with users).

"Silicon cycles will not disappear, but I think that their waves will become smaller, because huge investments and a long run (simultaneous development of three-generation DRAMs) will become necessary with the distinction of manufactured products. The number of enterprises having this ability will become limited. If the number of supply shares thus decreases, the silicon cycles will become moderate. There is a move toward oligopoly due to the distinction

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of manufactured products. I think that makers unable to make silicon cycles moderate are weak.

"As for international relations, we will reach an age of alliance and sharing. Having technological competitiveness is a key to resolving friction. Toshiba was able to cooperate with Motorola because Toshiba was strong in 1M DRAMs. Motorola was able to cooperate with Toshiba because Motorola was strong in microprocessors."

Kazuo Kanehara, Hitachi, managing director and leader of the electronic business group: "Makers should complement one another, making the most of their favorite techniques."

"For the past 10 years the Hitachi semiconductor business group has been attaining growth at the annual rate of 13-14 percent. From now on, too, it will be able to follow the same trend. To maintain this growth, we must pursue technological innovation rapidly, without delay. We will also make continuous investments.

"However, there is the problem that the efficiency of investments is dropping gradually. The higher the functions our products come to have, the more necessary it will be that these functions be recognized and that their prices rise. I think that the same is the case with sets (electronic apparatuses) and with semiconductors as well. Otherwise, the entire electronics industry will not improve.

"In the business field, we have the problem of coping with trade friction, and it will be essential for us to complement one another. Hitachi alone cannot deal with everything; manpower is insufficient. Each maker must make the most of his favorite sectors. In the case of the tie-up between Hitachi and VLSI Technology of the United States, for example, the design tool technology of that company and Hitachi's process technology were complementary.

"The efforts of ROK (Republic of Korea) makers to overtake us are also weighing on our minds. We must consider selling our intellectual property rights."

Takashi Kitaoka, Mitsubishi Electric Corp., executive director and manager of the electronic device business group: "We will increase our product series while narrowing our targets."

"After the previous depression, we formulated the following policies to stabilize our semiconductor business:

- 1) Increase the product series as much as possible.
- 2) Strengthen custom products.
- 3) Strengthen our financial constitution.
- 4) Establish a setup making it possible to cope with changes in the market.

"In increasing the series of manufactured products, we will specialize them to some extent. As for which custom products we should emphasize, we will deliver our products from profitable fields. We started with microcomputers, first of all. Since 1988, we have been concentrating on gate arrays and ASSPs. Our business efficiency is not good, but we will increase the rate of custom products to two-thirds. We want to lower the rate of such general-purpose products as memories from the preset 40-45 percent to one-third. Memories bring large profits but involve much risk.

"Looking at other industries such as textiles and iron and steel, we can see to some extent in what direction the semiconductor industry will move. History tells it. People's attitudes do not change in 5 or 10 years. Even when they do change, similarities do recur. We find various hints here and there. General electric machinery manufacturers have an advantage in that sense."

Junichi Mogi, Fujitsu, deputy leader of the electronic device business group: "We will adopt memories focused on ASICs."

"Fujitsu wants to focus its business development on ASICs all alone in the future. Even if we go on selling memory LSIs alone, an age will surely come when they will not sell. The market for memories is certainly larger than those for other devices. Memories may bring greater profits. In developing one's business, however, one will find it unsuccessful unless it is focused on ASICs.

"We want to avoid the practice of purchasing ASICs from Fujitsu while purchasing memories from other semiconductor makers. We will carry on business focused on ASICs and sell memories as well. We cannot sell memories alone.

"Fujitsu's strong point as to ASICs lies in its development environment. We were quick in making it possible to develop ASICs, too, through using 'personal computers' and workstations. I think we should have the expenses for this development paid. In a sense, the same can be said of software.

"Will the 1990's be an age of ASSPs? Will it not be an age when something flexible is added to them? An area is necessary to make customization possible for the sake of distinction. Otherwise, there will be no big difference in any set, even if the ASSP is used."

Tadashi Kubota, Matsushita Electronics Corp., managing director and leader of the first business group: "We will develop memories in anticipation of demand within Matsushita."

"Currently, the demand for memories within the Matsushita group is small. In the future, Matsushita also will start working on computers. For this purpose, it will increase the production of general-purpose memories for DRAMs and SRAMs. In addition, Matsushita has memories for images, and it must supply them to EDTV and HDTV. It will sell them outside the company, of course.

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"What are the strong points of the semiconductors of Matsushita Electronics Corp.? LSIs for VTRs, for example, are in steady use. Matsushita's VTRs are strong, and the LSIs for these VTRs are manufactured by this company. I think this is why these LSIs are sold to other VTR makers as well.

"Sets are discriminated in terms of functions and performance. This is software.

"It is hardly possible to make discrimination in terms of hardware. The added values of LSIs are not evaluated. Even if a circuit priced at ¥4,000, stored in a printed wire board, is included in a one-chip LSI and sold at a price of ¥2,000, another semiconductor maker may sell it at a still lower price. This would bring about low-price competition. I think such a process will not change in the 1990's, either.

"To get out of this cycle, there will be no other way for us but to manufacture products unique to the Matsushita Electronics Corp. Matsushita will defend itself from copying practices by means of its intellectual property right."

Takao Miura, Sanyo Electric, director, deputy leader of the semiconductor business group, and manager of the sales division: "All-purpose type business should be converted to a priority principle."

"Sanyo Electric Co. has so far promoted an all-purpose type of development of its manufactured products. In the 1990's, however, it will clarify its priority items. Enterprises having sectors that are superior in specific items are stronger than those dealing with all sorts of items. Enterprises having both strong and weak divisions can exchange technologies within themselves, but this is impossible within those having neither of these divisions. It is not that Sanyo Electric has had no priority items up to the present. It has not made such items clear, and therefore it may have appeared to have 'expanded without strategy.'

"Sanyo has been strong in bipolar analog technology. Practical use of analog ASICs is progressing little by little. It is impossible to deal with everything by means of digital ICs alone. I think we should strive hard with this point in mind. We intend to exert ourselves in the field of DSP, too, which processes signals through conversion from analog to digital signals.

"After the start of trade friction, the semiconductor industry has entered an age of harmony. Cooperation with overseas makers is important. We have been cooperating with Micron Technology of the United States in the sale of memory LSIs. We want to cooperate with foreign enterprises in fields other than sales, too. We will cooperate in overseas production as well. For this purpose, too, individuality is important."

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**Hiroashi Inoue, Sharp Corp., director and leader of its IC business group:**  
"Our development is focused on custom LSIs."

"Sharp is making business developments focused on custom LSIs. This will not change in the 1990's, either. As for memories, Sharp's production will be focused on masked ROMs. We regard them also as custom LSIs."

"Sharp did not come under direct attack at the time of the 1985-1986 depression, but we were not happy at all with the fall in the price of semiconductor products. Even when memories became insufficient after that, we did not pursue DRAMs. Sharp is steering its business so as not to suffer a swell of silicon cycles. If we are to deal with DRAMs, we would aim at products for exclusive use."

"It is said that custom LSIs hardly bring profits. However, I think this is due to lack of ingenuity. We are coping with matters in our own way as to manufacturing lines as well."

"In the future, sets themselves will be required to have the characteristics of a custom LSI. The age of mass sales at low price will come to an end. I think this trend will make progress. Articles wanted by end users will sell for reasons other than price. Both sets and semiconductors will bring due profits, and I think this must be the case."

**Yoichi Tanaka, Oki Electric Industry, director and manager of the electronic device business group:** "We will steadily follow the single path of DRAMs."

"DRAM in a sense constitutes a single path, and we must follow this path by all means. We are working on them on the premise that there will be silicon cycles of one degree or another. Our fundamental strategy did not change in the depression of 1985, either. We will not abandon this strategy even in depression."

"DRAMs are a driving force for technology. They can be pushed forward to 16M and then to 64M. Oki intends to join the top-level group. In light of the scale of our company, the investment for this purpose will be a big task, but we do not intend to give it up."

"Oki's fundamental strategy is to conduct memory, semicustom, and full-custom businesses at the rate of one-third each. This will not change in the 1990's, either."

"Carrying out memory business alone tends to bring a comparatively small profit, considering the amount of money spent for it. If Oki has technological ties with users in custom business, we will be able to expect them to prefer Oki in purchasing memories. It is important to have close ties with users."

"Semicustom business is also effective in cultivating our ability to make proposals to users. This is also connected with our sales of standard products for exclusive use."

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Osamu Furukawa, ROHM, director and manager of LSI group: "We will make the most of our strong point of being an exclusive maker of parts."

"The strong point of ROHM is that it is an exclusive maker of electronic parts. It can keep the secrets of set makers. This is reassuring for set makers having no semiconductor divisions. Even set makers having semiconductor divisions probably have no surplus power to handle everything.

"Technologically, ROHM has a history of manufacturing parts for bipolar analog ICs. Recently it is making preferential efforts for parts connected with microcomputers and digital ASICs. ROHM must attain an annual average growth rate of 10-20 percent in the 1990's.

"ROHM will continue the development of manufacturing processes, reducing the size to 0.8  $\mu\text{m}$ , 0.6  $\mu\text{m}$ , and 0.5  $\mu\text{m}$ . It wants to keep pace with major semiconductor makers. Its investment will increase, but prices cannot be determined in a simple way.

"It was for the following two purposes that ROHM began its memory business during the latter half of the 1980's: One was to sell semiconductors through spinoffs—SRAMs and masked ROMs; the other was to expand a new market for EEPROMs. Even if ROHM edges itself into the market for advanced DRAMs the way major manufacturers did, it would find it difficult to attain success."

Shosukie Shinoda, NMB, managing director: "The most advanced technology is our basis."

"NMB has reached the present stage because it has improved its manufacturing technique. It can make the best use of the most advanced memories as a technology driver. It will go on producing high-speed DRAMs. It can produce other kinds of LSIs as well. NMB can produce composite memories, too, with DRAMs as the core. We think that our tie-ups on OEMs, joint development, etc., will take beneficial forms.

"Manufacturing techniques are extremely important. Making investments is a great task, but not impossible. Problems involved in such techniques cannot be solved with money alone. Accumulation of techniques and sensible technicians are necessary; it is rather easier to collect funds. Money cannot buy the skillful manufacture of the most advanced products.

"Because of the last depression, the semiconductor industry will change to some extent, although this depends upon the attitudes of various companies.

"Some kind of controls must be instituted to prevent a rapid change in price. Makers and users should assemble and make medium- or long-term promises covering five years or so, each bringing his own outlook. Furthermore, sharing will take place to some extent, taking advantage of various semiconductor companies' specialties."

Abbreviations in this special edition (in alphabetical order)

ALU: arithmetic logic unit  
ASIC: application specific integrated circuit  
ASSP: application specific standard product  
CMOS: complementary metal-oxide semiconductor  
CAD: computer aided design  
DRAM: dynamic random access memory  
ECL: emitter coupled logic  
EEPROM: electrically erasable programmable ROM  
EPROM: erasable programmable ROM  
EWS: engineering workstation  
FET: field effect transistor  
FMV: fair market value  
HDTV: high-definition television  
IC: integrated circuit  
LSI: large-scale integrated circuit  
MIPS: million instructions per second  
MOS: metal oxide semiconductor  
MSI: medium scale integrated circuit  
NIES: Newly Industrializing Economies  
OTP: one time programmable ROM  
RAM: random access memory  
ROM: read-only memory  
SOJ: small outline J-leaded package  
SRAM: static random access memory  
SSI: small scale integrated circuit  
TAB: tape automated bonding  
TSOP: thin small outline package  
TTL: transistor transistor logic  
ULSI: ultra large-scale integrated circuit  
VLSI: very large-scale integrated circuit

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## Part 3. Memory Capacity Will Continue To Expand Fourfold Every 3 Years, but the Trends of Prices and External Specifications Will Change

In the 1990's, the memory capacity of DRAMs will expand fourfold every three years, as has been the case to date. In the 2000's, 1G-bit samples will reach users; however, prices and specifications will differ from current trends. Beginning with the age of 1M-bit DRAMs, the per-bit price will drop more slowly. The per-chip price will roughly double with each new generation. The standard package will become larger and larger. To increase the packaging density at the same rate as hitherto, it will be necessary to elaborate a new plan. Such trends will work in the direction of preventing products from shifting to larger capacities. In an age when 64M-bit products are used widely, they will coexist with 1M-16M-bit products.

Table 1. DRAMs in the 1990's

Year	1990-91	1993-94	1996-97	1999-2000
Generation reaching largest scale of mass production (bit)	1M	4M	16M	64M
Design rule ( $\mu\text{m}$ )	1.2	0.8	0.5	0.3
Generation reaching full-scale production (bit)	4M	16M	64M	256M
Generations of coexistence (bit)	256K 64K	1M 256K	4M 1M 256K	16M 4M 1M
Main external specifications in generation of largest-scale mass production				
Access time (ns)	100	80	60	40-60
Address	Multiple	Multiple	Multiple	Non-multiple/ multiple 3.3
Power source voltage (V)	5	5	5 (internal voltage drop)	
Package width (mil)	300	350/300	400	600
Bit structure	X1/X4	X1/X4/X8	X1/X4/X8/ X16	X1/X4/X8/ X16/X32
Per-chip price (¥)	600-800	1,200- 1,600	2,400- 3,200	4,800- 6,400 (7,200- 9,600)
two-fold every generation (threefold every generation)				

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DRAMs, which have been pulling the semiconductor industry as well as the semiconductor memory market with their high integration density and low price as weapons, will push their way to a larger capacity in the 1990's as well (Table 1). Semiconductor makers say unanimously, "It will be possible for the memory capacity to keep the fourfold expansion pace every three years."

At this pace, the mass production of 256M bit DRAMs will begin on a full scale in 1990 (monthly production per maker: 1 million DRAMs or more). Around 2000, makers will receive 1G-bit engineering samples.

However, the trends except for memory capacity will change markedly.

First, the price will not fall at the same pace as previously. If the memory capacity increases fourfold, the unit price of chips will rise. The per-bit price will fall, but it will not be one-fourth that in the preceding generation, as has been the case up till now.

If the per-chip price remains constant (if the per-bit price is one-fourth that of the preceding generation), "it will be impossible to make continuous investments to mass-produce DRAMs for the next generation" (Kazuo Kanehara, Hitachi, managing director and manager of its electronic business group). With the lapse of a generation, that is, each time the memory capacity increases fourfold, the per-chip bottom price will rise about twofold. One semiconductor maker even says that when 64M-bit products appear, even a twofold rise in the bottom price will cause him difficulty, and that the per-chip price may rise further.

This price rise will not be limited to DRAMs. The same will be the case with other kinds of memory LSIs manufactured with the same microprocessing technology.

In the 1990's, external specifications will change every generation.

The 4M products will be the first to become large in package size, followed by 16M and 64M ones. As a result, the increase in package density will slow down. Even when the memory capacity increases fourfold, the package density will not show the same rate of increase.

As for bit structure, the number of X8-bit articles will increase in the case of 4M DRAMs, in addition to X1/X4-bit articles. Among 16M DRAMs, X16-bit articles will appear.

The power source voltage will be 5 V up to 16M DRAMs, but it will drop to 3.3 V in the case of 64M DRAMs.

With the shortening of address-access time, high-speed products with non-multiple addresses will be specialized among 64M DRAMs.

With the expansion in the capacity of general-purpose DRAMs, the rate of DRAMs for exclusive use will rise, with optimum functions attached to their uses.

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These phenomena will delay their shift to products of larger memory capacity. Thus they will cause an increase in the number of DRAMs produced with the same capacities.

### DRAMs Covering Many Generations Will Coexist

Full-scale mass production of 4M-bit DRAMs will begin in 1990-91. Small outline J-leaded package (SOJ) is the main package, in two sizes—one measuring 300 mil wide and the other measuring 350 mil. As for bit structure, X8-bit products will begin to appear in addition to X1/X4-bit ones. The access time is 80 ns in the main.

Around this time, 1M-bit DRAMs will be mass produced in the largest scale. The per-chip price will settle down to about ¥600-800. The 64K-bit products will also remain, though in small quantities. Four generations of DRAMs ranging from 4M-bit to 64M-bit DRAMs will coexist in the market.

In 1993-94, mass production of 16M-bit articles will get going, and the width of a package will increase to 400 mil. To increase the package density, a thin small outline package (TSOP) about 1 mm thick will be widely used.

As for bit structure, X16-bit articles will also appear. The main access time will be 60 ns.

Around this time, the scale of mass production will be the largest in the case of 4M. If the bottom unit price of chips rises twofold every generation (by the so-called bi-rule<sup>1</sup>), the per-chip price of 4M DRAMs will be ¥1,200-1,600. About this time, 64K DRAMs will disappear, and four generations of DRAMs ranging from 16M to 256K (64K x 4) will coexist in the market.

The mass production of 64M-bit DRAMs will begin in 1996-97. Here the power source voltage will drop from 5 V to 3.3 V, and the access time will shorten to 40-60 ns. The 40 ns products will become nonmultiple in address and they will be differentiated from multiple-address products. The width of SOJ packages will further increase to 600 mil.<sup>2</sup> To improve the package density, an increasing number of users will adopt bare packages in addition to TSOPs. As for bit structure, X32-bit products may appear.

The unit price of chips for 16M-bit DRAMs, which will become the major products around that time, will be about ¥2,400-3,200. We wonder if 256K will disappear. The 64K x 4-bit DRAMs may remain deep-rooted. If so, five generations of products ranging from 64M to 256K will coexist in the market.

In 1999-2000, 256M-bit DRAMs will be mass produced in full scale, with the power source voltage maintaining 3.3 V.

In this period, 64M-bit DRAMs will be mainly produced, and the unit chip price may be about ¥4,800-6,400. If the chip price rises threefold, it will be ¥7,000-10,000. The 1M (256K x 4) products will still remain. Thus, products covering five generations, ranging from 256M to 1M, will coexist in the market.

### Unit Chip Price Will No Longer Remain Constant

An increasing bit demand that roughly doubled annually from the 1970's to the first half of the 1980's supported the popular notion that 1) memory capacity increases fourfold every three years and that 2) the unit price of chips is constant (Figures 1 and 2).

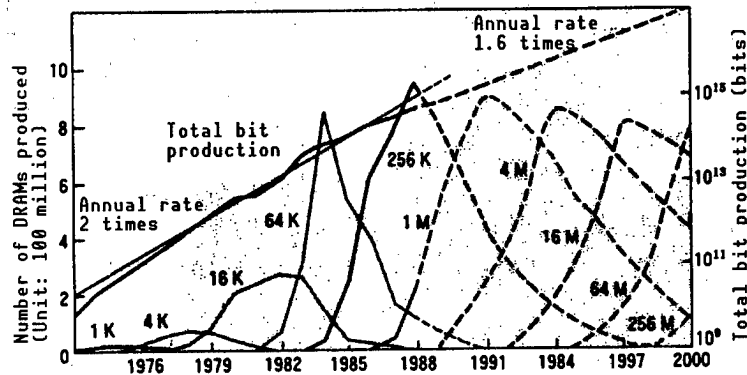


Figure 1. Changes in Number of DRAMs Produced and in Total Bit Demand

DRAM production increases markedly with the progress of generation change from the 4K bit to the 16K bit and then to the 64K bit. Thus, total bit production doubled annually. However, this changed with the semiconductor depression in 1985-86. The maximum number of 256K bit DRAMs produced was generally the same as that of 64K bit DRAMs. Total bit production has slowed to an approximately 1.6-fold annual increase. (Figures through 1989 are based on the data of Dataquest Inc. of the United States, and those from 1989 are estimated by NIKKEI ELECTRONICS.)

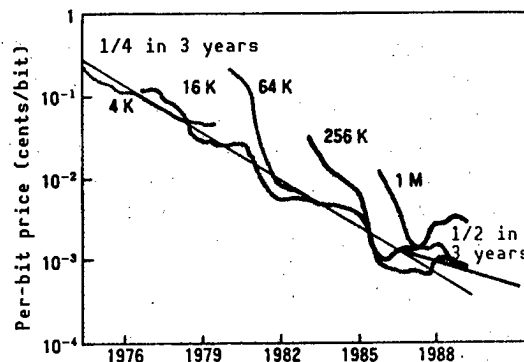


Figure 2. Changes in Per-Bit Price of DRAMs

The per-bit price up to 256K-bit DRAMs dropped at the pace of one-fourth each time a three-year generation was replaced by the next three-year generation (with the unit-chip price unchanged in each generation). The pace at which the per-bit price dropped slowed down to more than half in three years. (Figures are based on the data of Dataquest Inc. of the United States.)

This "myth" began to collapse from the time of the semiconductor depression in 1985-86, when the unit prices of 64K and 256K chips fell suddenly. After this bitter experience, many semiconductor makers became cautious about investments. In 1987-88, when demand moved toward recovery, DRAMs were very insufficient. For more than two years, 1M chips were priced at ¥2,000, partly because of the political factor attending a Japan-U.S. semiconductor agreement.

#### Makers Have Difficulty When Bi-Rule Is Not Adopted

In the view of semiconductor makers, the unit price of DRAM chips in the 1990's is certain to rise every generation, because investments in development and facilities and operating costs will increase with progress in the micronizing of manufacturing techniques, as the size is reduced from 0.8  $\mu\text{m}$  to 0.5  $\mu\text{m}$ , 0.3  $\mu\text{m}$ , and to 0.2  $\mu\text{m}$ .

"In light of the manufacturing cost, it is impossible to continue investments in the mass production of next-generation DRAMs unless the unit-chip price is doubled every generation (bi-rule). This will not change, no matter how greatly the demand may increase," says NEC director General Sasaki. There is also the view that the unit-chip price will rise further in the latter half of the 1990's. Hitachi executive director Kanehara says, "We do not want to fix such a constant as a twofold increase. We want to avoid a state in which the per-bit price does not fall even when a generation is replaced by the next generation, but in the latter half of the 1990's, the situation will make it more and more difficult for the price to fall."

On the other hand, someone else takes the view that "the price competition among makers will serve as a factor reducing the unit price of chips" (Tecsel representative director Shoji Akutsu). "There is still no one who has truly grasped the manufacturing cost. It is impossible to ascertain whether the unit price of chips will rise enough to actually follow the bi-rule" (Shoji Akutsu).

If supply and demand become tight, the unit-chip price will more than double every generation as expected by makers. In the case of 4M-bit DRAMs, on the other hand, there are signs that supply will far exceed demand. In such major semiconductor makers as Toshiba and Hitachi, mass production of 4M-bit DRAMs is already under way. With the progress of low-price competition, there is the fear that the "tragedy of 256K" may be repeated in 4M. The breakwater to prevent this is the FMV (fair market value) under the Japan-U.S. Semiconductor Agreement. However, semiconductor makers outside the agreement threaten to trigger price competition.

#### Growth of Memory Capacity Employed by Users Will Slow Down

It may be favorable for users if the price of 4M-bit DRAMs drops to a low level. However, a "tragedy of 4M" might bring about in 16M the same result as in 1M, because the oligopolistic trend is expected to progress. The price competition among makers will weaken, and the unit price of chips for 16M will not fall (Figure 3). Thus, the consequences will be the same, except that fluctuation will become extreme.

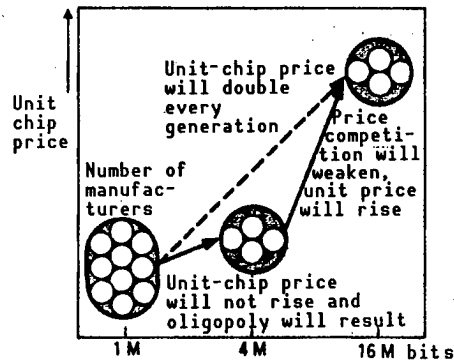


Figure 3. Unit Price of Chips Will Rise, After All

In the case of 4M-bit DRAMs, mass production by makers is under way, and another drop in unit-chip price due to oversupply cannot be ruled out. But if such a situation arises, the number of makers capable of making continuous investments in 16M-bit DRAMs will be narrowed, and thus an oligopolistic trend among DRAM makers will gain strength. As a consequence, price competition among them over 16M-bit DRAMs will weaken, and the unit price of chips will rise again.

Looking over the 1990's, it is likely that the unit price of DRAM chips will more than double (per-bit unit price: more than one-half) each time the memory capacity increases fourfold.

How will users react to this? One response says, "We will definitely use those manufactured products that lead end users to recognize their added values even more than the price rises caused by increases in memory" (major printer maker).

However, many makers are of the following opinions, "If the pace of a drop in per-bit price slows down, the increase in per-system memory capacity will also slow down to that extent" (Fujitsu staff member in charge of mainframes). "We do not want to raise the prices of final manufactured products. We will expand the memory capacity within a limit where the memory price will settle at a certain level" (major facsimile maker).

#### Increasing Package Density Will Become Difficult

Packages gradually become larger from the stage of 4M (Figure 4), because LSI chips increase too much in size to be accommodated in the packages used so far.

The first-generation products of Toshiba and Hitachi, which are going ahead in the mass production of 4M-bit DRAMs, are packaged in plastic SOJ 350 mil wide. This is larger than the width of 300 mil for 1M-bit DRAMs. Both companies will supply articles sealed with 300-mil SOJs for a reduced version of second-generation DRAMs.

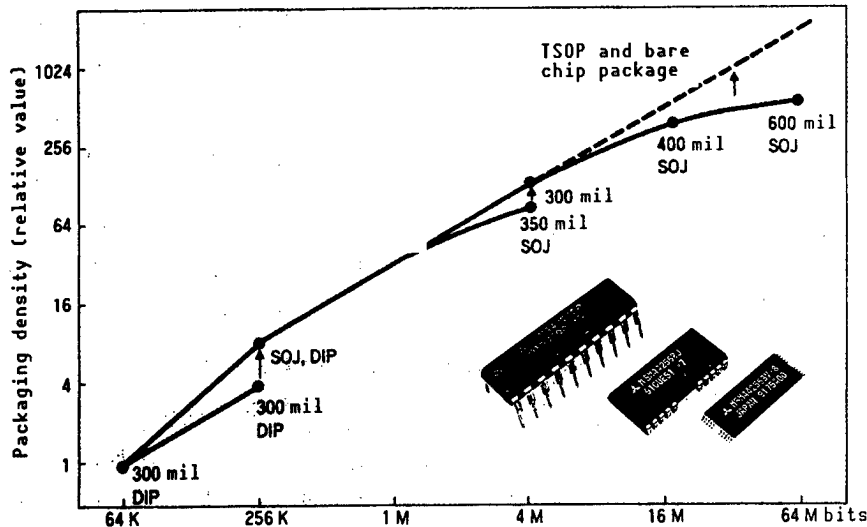


Figure 4. Increasing Package Density Will Become Difficult

The chip area for DRAMs has been expanded about 150 percent each time the memory capacity has increased fourfold. At the stage of 16M, it will become impossible for the chip to be housed in an SOJ package 300 mil wide. Even if the memory capacity increases fourfold, it will become impossible for packaging density to rise fourfold. Packaging technologies included those for TSOPs about 1 mm thick each and bare chip packages will spread more widely than ever.

In the case of 16M DRAMs, the width will still increase to 400 mil. For 64M DRAMs, it is likely to increase to 600 mil. Even when the memory capacity is fourfold, the package density will not rise more than 250-300 percent. If a second-generation DRAM appears with a reduced chip area, the package may not become so large, but it is certain that the package density will not readily rise.

Consequently, in order to raise the packaging density, it will become necessary to create a new packaging technology. If, for instance, an extremely thin package (TSOP) about 1 mm thick is adopted, it will be possible to further raise the packaging density by directly loading a base plate with a chip (bare chip packaging).

"The packaging area influences the performance of the mainframe as well. If the problem of reliability can be settled, we would like to investigate it by all means" (Fujitsu information system business group). "We will have to give serious thought to it from now on" (major facsimile maker).

#### Power-Source Voltage Will Change at the Stage of 64M

The power-source voltage, which became only 5 V in the 64K age, will drop to 3.3 V in the 64M age (Figure 5) because of the need for maintaining reliability and holding down an increase in power consumption.

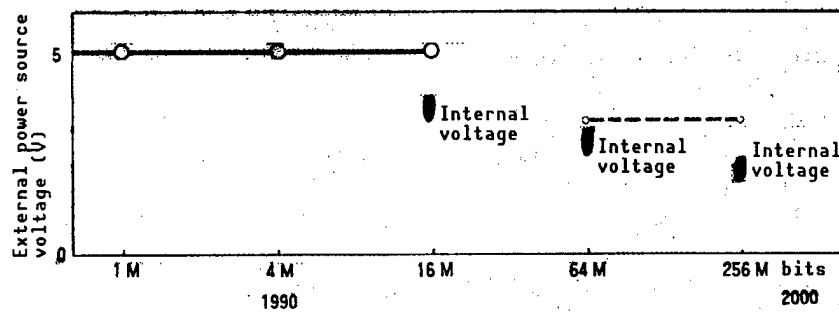


Figure 5. Power-Source Voltage Will Drop at the Stage of 64M

Since the 64K-bit age, DRAMs have been maintaining a power-source voltage amounting to only 5 V. In the age of 16M, however, the internal power source will have to be dropped to 3.3~4.0 V, though the external power source can be retained at 5 V, for the purpose of maintaining reliability and power consumption. At the stage of 64M, the external power source will drop from 5 V to 3.3 V.

Makers will manage with 16M products using the external voltage of 5 V and the internal voltage of 3~4 V. When it comes to 64M, however, they will find it difficult to work out a method to drop the internal voltage. What about 256M? Users have the following expectation, "We know that the power source voltage must be dropped, but we want the external voltage to be kept at the same level at least for two generations" (Hitachi computer business group). "In the case of 256M, too, it will be possible to keep the external power source voltage at 3.3 V by dropping the internal voltage" (Toshiba DRAM designer).

#### Nonmultiple Address, High-Speed DRAMs Will Coexist

To date, the access time of DRAMs has been shortened every generation, with the memory capacity expanded at the same time (Figure 6). It is likely that this trend can be maintained up to 64M. If so, the access time of 64M will be shortened to 40 ns. This will make the multiplication of address difficult. "Address multiplication will be limited to 50 ns" (NEC, etc.). "As a matter of fact, 60 ns will be the shortest access time that can be achieved, won't it?" (Mitsubishi Electric). DRAMs with 40 ns access time will be unusable unless the address is made nonmultiple.

Of course, it is not that the nonmultiple address formula will be adopted for all 64M DRAMs. "We want to continue to use medium-speed products, too, for which we do not adopt the nonmultiple address formula" (Hitachi computer business division). Thus, nonmultiple address high-speed products will come to coexist with multiple address products involving 50~60 ns access time.

#### Specialization Will make Further Progress

If the DRAM capacity becomes increasingly large, there will be increasing uses for necessary memory capacities to be accommodated in several chips. In that case, system designers will come to have strong hopes for products for exclusive use.<sup>4,5</sup>

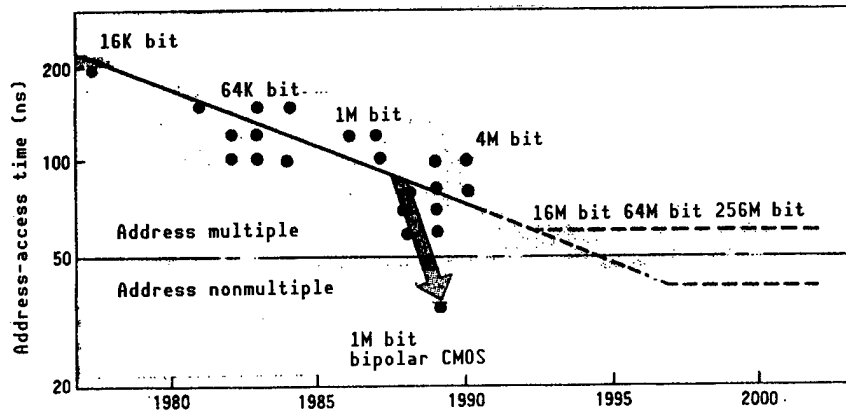


Figure 6. Changes in the Access Time of DRAMs

The access time of DRAMs has been shortened with the memory capacity expanded at the same time. In the age of 64M, the access time will become 40 ns. If the access time is shortened to this extent, it will be impossible to use the multiple address formula, and the address will become nonmultiple.

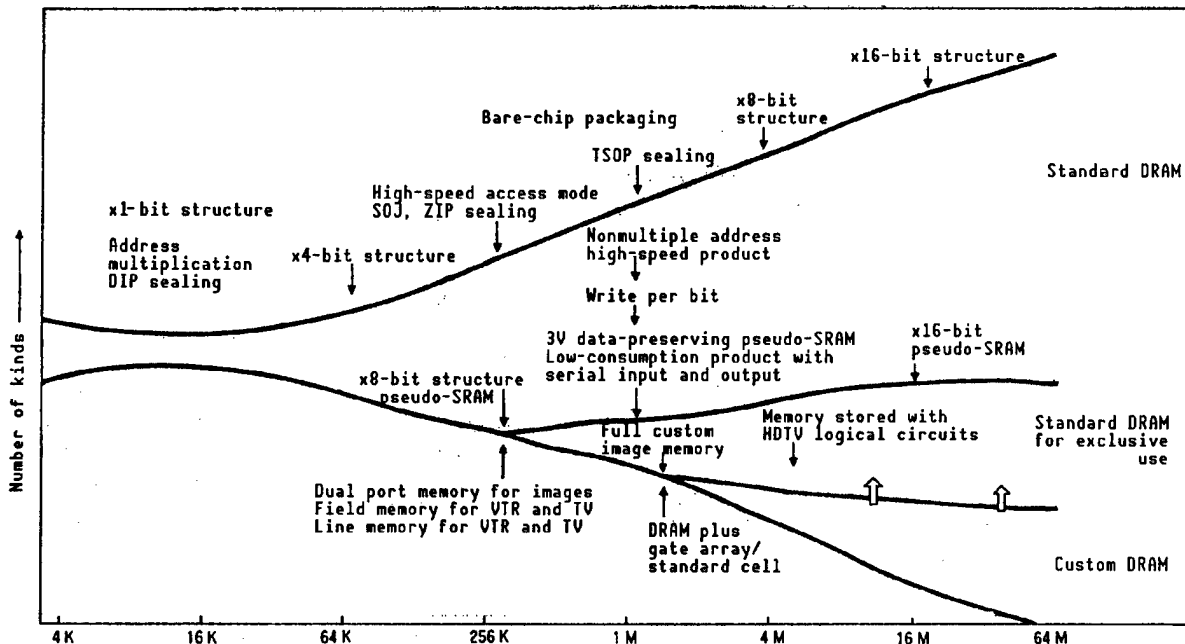


Figure 7. Diversification and Exclusive Use of DRAMs Will Progress

Since the use of 256K DRAMs in the 1980's, the diversification of standard DRAMs has made progress in high-speed access mode, packaging, bit architecture, etc. DRAMs for exclusive use have also appeared. With an expected increase in the capacity of standard DRAMs in the 1990's, the diversification of these DRAMs will make still more progress. At the same time, the percentage of DRAMs for exclusive use will become higher.

DRAMs for exclusive use appeared in the mid-1980's and will continue to multiply in the 1990's; the percentage of such DRAMs will increase (Figure 7). "Their rate will increase to 10 percent in 1992 and to 25-30 percent in 1995" (Oki Electric Industry).

Makers will come to furnish users with DRAMs for exclusive use more aggressively than ever. "In the 1990's, when the per-bit price is not expected to drop so readily, makers will be obligated to furnish users with DRAMs for exclusive use equipped with functions meeting their needs" (Hitachi semiconductor business division). "To the demand for DRAMs, too, we will make positive efforts to develop products of optimum use" (Takashi Kitaoka, Mitsubishi Electric Corp. executive director and manager of its electronic device business group).

Demand for DRAMs for exclusive use is strong in the field of image processing. In the case of digital TV, for example, 2M-, 4M-, and 8M-bit image memories are highly desirable. "We want to achieve a system-on-chip structure, with signal processing circuits also loaded. If the memory capacity is increased at random, the products will be unusable" (major maker of electric appliances for home use).

In the 1990's, the main memories for personal computers also will not be unaffected by this trend toward specialization. In the age of 16M-bit DRAMs, the main memory will come to be put in one or two chips in the case of small-scale systems. Mitsubishi Electric Corp., for example, has recently manufactured a DRAM stored with a cache memory, with an eye on that age.<sup>5</sup> This was created by putting on one chip a memory hierarchy consisting of the cache memory and the main memory. A DRAM exclusively used for the main memory of such a small-scale system will also be developed in the future.

[Boxed item, p 131]

#### Capacity of General-Purpose SRAMs Is on the Increase for High-Speed Products and Those Involving Low Power Consumption

The general-purpose SRAMs currently on the market are on a 16K-1M level. The output of 256K SRAMs has exceeded that of 16K SRAM for the first time this year. Many users say, "We want to continue to use 16K and 64K SRAMs for any length of time" (major facsimile maker). In contrast to DRAMs, alternation of generations does not readily take place. Makers are supplying four generations of general-purpose SRAMs to the market by dividing roles among themselves, with some focusing on small-capacity SRAMs and others emphasizing large-capacity products. This trend will continue in the 1990's.

General-purpose SRAMs are grouped into high-speed articles with access times of 50 ns or less and medium-speed ones with an access time of 50 ns or longer. Further, the medium-speed SRAMs are divided into products consuming electric current amounting to less than 10  $\mu$ A during waiting time and those consuming 10-100  $\mu$ A.

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In the 1990's, general-purpose SRAMs will be narrowed down to high-speed and medium-speed products consuming small amounts of electric current. "Medium-speed SRAMs that consume more than 10  $\mu$ A during waiting time will be replaced by pseudo-SRAMs" (Hitachi semiconductor business division).

The capacity will be increased at the same rate as previously. At the end of the 1990's, the mass production of 64M-bit SRAMs will get under way.

Since the appearance of 256K-bit and 1M-bit products in the latter half of the 1980's, the period from the marketing of medium-speed products to that of high-speed ones has rapidly shortened. In the case of 1M-bit products, for example, the period was only 1 year. This trend will continue in the 1990's as well, and it will become possible for high-speed products and medium-speed ones consuming small amounts of electric current to be obtained almost at the same time.

Semiconductor makers take the view that the access time of SRAMs on a 256K bit or a higher level is limited to 10-12 ns when the input and output of signals are on the transistor transistor logic (TTL) level. The speed will be increased further by putting the input and output on the emitter coupled logic (ECL) level through the use of bipolar CMOS technology.

[Boxed item, p 132]

### Mask ROMs May Enter a G-Bit Age in Late 1990's; Attention To Be Paid to Flush EEPROM and NAND EEPROM

Mask ROMs, having the largest memory capacity among semiconductor memories, will enter a G-bit age in the late 1990's, if the capacity is increased at the current rate. For this purpose, it is necessary to reform the redundant circuit technology designed to remedy manufacturing defects, and the memory cell structure.

What about the EEPROM to erase memory contents by applying ultraviolet rays? If things go smoothly, the mass production of 256M-bit products will be started in the late 1990's as in the case of DRAMs.

What is to be noted is the flush EEPROM that appeared in the 1980's.<sup>6</sup> At present, 1M-bit products are on the market. Partly because it is not long since they appeared as manufactured products, their memory capacity is lagging one generation behind that of EPROM.

However, when the same manufacturing technology is used, the chip area for flush EEPROM can be held down to 10-20 percent more than that for the ultraviolet erasure EPROM. If products having the same capacity as the most advanced EPROM appear in the 1990's, "We will replace a fairly large number of EPROMs and OTPs with them" (Oki Electric Industry), making the most of their characteristic of being electrically erasable.

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Products capable of erasure not only in bulk but also in units of several K bits and those capable of operations with a single power source do not contribute to reducing the unit price of chips. They will not become the mainstream in the 1990's, either.

As for the EEPROM that is reloadable in units of byte, the mass production of 64M products will get under way in the late 1990's.

Besides, the trend of EEPROMs of NAND construction, developed by Toshiba last year, is of great interest.<sup>7</sup> Their characteristic is that the size of the memory cell can be reduced to one-third that of a DRAM. In terms of chip area, it is possible to reduce the price to the same level as a mask ROM.

Although the access time is as long as several  $\mu$ s or so, they might replace magnetic memories through making the most of their characteristic of being reloadable, inexpensive, and nonvolatile memories.

[End boxed items]

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2. Yamaguchi and Mochizuki, "LSI Technology Pressed for Another Qualitative Change," Ibid., August 1989, pp 42-50.
3. Miyazaki, "Memories in an 0.5  $\mu$ m Age: Trade-Off Between Reliability and Speed as to Internal Power Source," Ibid., October 1989, pp 91-95.
4. Matsunaga, "DRAMs for Exclusive Use Strengthening Custom Trend," NIKKEI ELECTRONICS, No 440, 2 May 1988, pp 120-125.
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6. Masuoka, "256K-Bit EEPROM Aimed Even at Replacing Ultraviolet Erasure-Type EPROM," Ibid., No 374, 29 July 1987, pp 195-209.
7. Iboh, Y., Momodomi, M., Shiroto, R., Iwata, Y., Nakayama, R., Kirisawa, R., Tanaka, T., Tomita, K., Inoue, S., and Masuoka, F., "An Experimental 4 Mb CMOS EEPROM with a NAND Structure Cell," 1989 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE (ISSCC), DIGEST OF TECHNICAL PAPERS, Speech No. THAM 10.4, pp 134-135.

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### Part 4. Only a Limited Number of Professionals Will Benefit From Silicon Compilation for LSI Design

In the latter half of the 1990's, it will be possible to make automatic designs for the most advanced custom LSIs from chip specifications by using silicon compilation. However, the dream computer aided design (CAD) tool will be restricted by such factors as the slowdown of the fall in Si price (per unit function). Actually, the users (set makers) benefiting from this tool are unexpectedly few. On the other hand, the number of semiconductor makers capable of furnishing advanced processes is also limited for such reasons as the increase in the amount of facilities investments. Therefore, it is likely that the field of the most advanced custom LSIs will be created only by a limited number of makers and users.

The scope of automatic designs using silicon compilation ranges from specifications for desired LSIs to mask patterns, making it possible to create standard-cell LSIs for the most advanced processes. Thus, advanced custom LSIs will reach users (set makers) instantly. Such a story will become real in the latter half of the 1990's.

However, users who can play a part in this story are not as many as expected. The same is the case with semiconductor makers. This is because a situation that can be called "a counterattack by Si" may arise.

For example, the assumption in this story, to the effect that the Si price will limitlessly approach zero, will collapse. Also, the expectation that digital circuits can be designed by stacking them together is likely to be upset. Consequently, the silicon compilation will be subjected to restrictions, and it will become a tool for a limited number of professionals rather than for everyone. Like a sharp-edged tool, this will produce an excellent result if it is used skillfully, but it may cause injury if used by a nonprofessional.

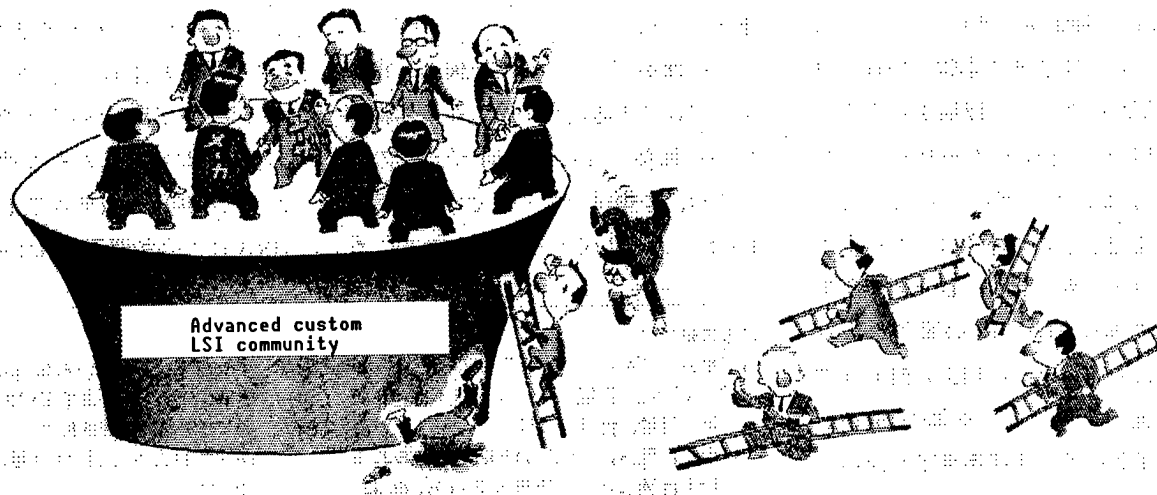
If users are few, competition between semiconductor makers will become severe, and it will also become difficult to adjust the manufacturing technology and design environment that differentiate one company from another. This may cause some semiconductor makers to drop out. If the ability to supply advanced custom LSIs declines, the number of users whom semiconductor makers can deal with will become limited, and only those users beneficial to semiconductor makers will remain. Thus, the world of advanced custom LSIs in the 1990's will form a community with high access barriers (Figure 1).

### Seeds of General-Purpose Products Are Sought Through Custom LSIs

In the eyes of users, ICs are among the means (HOW: how to manufacture) of realizing desired specifications (WHAT: what to manufacture). (HOW and WHAT, when mentioned hereafter, are to be viewed from the position of users.)

To date, semiconductor makers have been supplying ICs to users not as a mere means but as an attractive means. With a rise in the degree of integration from the level of ICs to that of LSIs and VLSIs, their role for sets has

Users (set makers) sought by semiconductor makers	Users (set makers) whom semi-conductors keep at a distance
<ul style="list-style-type: none"> <li>▷ Rich in WHAT (seeds of general-purpose LSIs)</li> <li>▷ Able to master silicon compilation</li> <li>▷ Issue orders for large quantities of custom ICs</li> <li>▷ Consume large amounts of memories</li> </ul>	<ul style="list-style-type: none"> <li>▷ Short of WHAT (seeds of general-purpose LSIs)</li> <li>▷ Unable to master silicon compilation</li> <li>▷ Issue orders for small quantities of custom ICs</li> <li>▷ Do not consume many memories</li> </ul>



Semiconductor makers sought by users (set makers)	Semiconductor makers whom users (set makers) keep at a distance
<ul style="list-style-type: none"> <li>▷ Equipped with microprocessing technology</li> <li>▷ Have silicon compilation</li> <li>▷ Rich in package articles</li> <li>▷ Have many support personnel</li> <li>▷ TAT is short</li> <li>▷ Unit price of chips is low</li> </ul>	<ul style="list-style-type: none"> <li>▷ Lacking microprocessing technology</li> <li>▷ Have no silicon compilation</li> <li>▷ Produce poor package articles</li> <li>▷ Have few support personnel</li> <li>▷ TAT is long</li> <li>▷ Unit price of chips is high</li> </ul>

Figure 1. Only a Limited Number of Users (Set Makers) and a Limited Number of Semiconductor Makers Will Take Part

In the latter half of the 1990's, it will become possible to make designs for standard cells of the building-block type for the most advanced processes. However, users and makers benefiting from these will not be so numerous as expected.

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become greater. Currently it is rather difficult to find sets not using ICs. In the 1990's, too, ICs will invariably be an indispensable means for sets.

What is wanted by users most intensely for LSIs is HOW for individual users' products, i.e., "custom LSIs." When they use these LSIs, they can easily differentiate their sets from those of other companies. However, the expenses for developing these LSIs are so high that they cannot easily benefit from them.

On the other hand, semiconductor makers want to supply HOW that can be commonly used by many users, i.e., "general-purpose LSIs." This is because production efficiency is so high in the case of articles to be mass produced that they are lucrative. They want to sidestep custom LSIs that are produced in small quantities. In spite of this, semiconductor makers cannot get away from custom LSIs, because "WHAT is always on the side of users" (independent design houses).

They cannot create general-purpose products without knowing WHAT. It can be said that for semiconductor makers, a custom LSI is like an antenna shop to pick up the seeds of lucrative general-purpose LSIs. A number of semiconductor makers say definitely, "To put it bluntly, we do not need to profit from custom LSI business."

If semiconductor makers had limitless development power, and if users were also able to make limitless investments in development, semiconductor makers would undertake all kinds of HOW and thus furnish custom LSIs to users. In reality, the two parties have been sharing HOW as if making a compromise.

### Heading Toward an Age of Semicustom LSIs

The currents of ICs leading to differentiation of sets are summed up by decades in Figure 2, starting from the 1960's. In the 1970's, the age of LSIs was reached, and microprocessors and memories appeared.<sup>1</sup> At this stage, semiconductor makers undertook microprocessors, memories, and development tools (these are also furnished by special makers in many cases) in terms of HOW (Figure 3). On the other hand, programs were developed by users. Thus, the HOW of the two sides jointly achieved WHAT for users.

With the advent of the 1980's, the micronizing of semiconductor processors progressed, and both microprocessors and memories made remarkable progress. With the improvement in the performance of microprocessors, for example, the processing ability of computers has improved rapidly. However, the number of sets consisting mainly of microprocessors and memories increased too much, and it became difficult to make distinctions among them without some other elements.

The requirement for this was met by gate arrays. Gate arrays are typical "semicustom LSIs." In other words, users and makers shared in the development of these LSIs. Thus, users' share in HOW extended to LSIs (Figure 3). In the age of microprocessors, LSI development had been undertaken by semiconductor makers.

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	1960's	1970's	1980's	1990's
IC scale	SSI, MSI	LSI	VLSI	ULSI
IC function	Standard logic IC	Microprocessor and memory	Gate array	Building block type standard cell
Development tool	Breadboard	Microcomputer development tool	EWS-based CAD system	Silicon compilation
HOW expression form under users' charge	Circuit diagram (hardware)	Program (software)	Net list (hardware)	Operational description (software)

Figure 2. Changes in ICs Leading to Differentiation of Sets

The age of semicustom LSIs came in the 1980's. The computers using CAD tools changed from the batch type, including large computers and minicomputers, to the interactive type such as EWS. Due to the expansion of the IC market, both development tools and CAD tools were dealt with by expert makers independently of semiconductor makers.

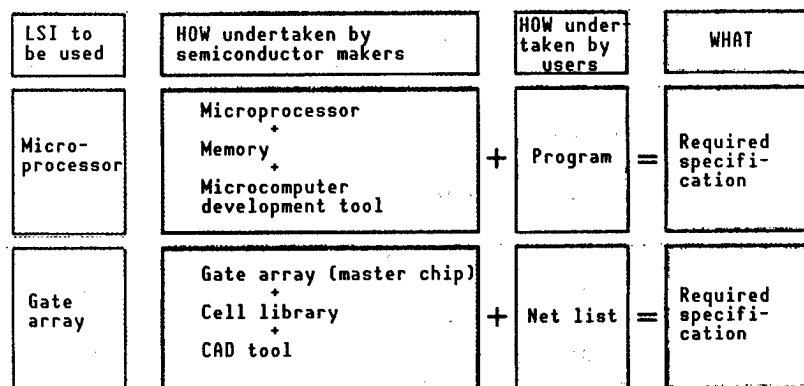


Figure 3. Share in HOW

The semiconductor side (including some makers specializing in development tools) and the user side (set makers) share in HOW and achieve users' WHAT (required specifications). Through the appearance of semicustom LSIs including gate arrays, users' share extended to LSIs.

Gate arrays, riding on the wave of the so-called "ASIC boom" in 1985, spread at a stretch.<sup>1</sup> The ASIC boom occurred because both semiconductor makers and set makers were forced to compromise (Figure 4).

In other words, semiconductor makers, faced with the memory depression, were compelled to reconsider their wholehearted devotion to memories and moved from general-purpose LSIs to semicustom LSIs. On the other hand, set makers,

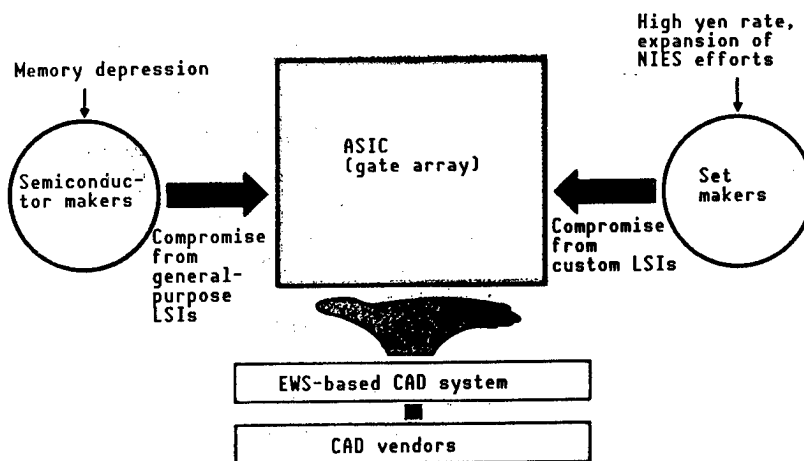


Figure 4. Structure of the ASIC Boom

The ASIC boom, occurring in 1985, resulted from both semiconductor makers and users (set makers) being forced to convert from the conventional structure. Both sides sought a compromise plan for semicustom LSIs (actually gate arrays). This was backed by the EWS-based CAD system. The semicustom LSI boom gave rise to many CAD ventures in the United States.

including those of machinery and equipment for public use, for example, were pressed to switch priorities from cost to higher added values, because of the high yen value and Newly Industrializing Economies' (NIES) expanding influence. They focused on shortening the period of development (favored in full-custom LSIs) rather than reducing the chip area (favored in semicustom LSIs). "To date, the United States has expected CAD to shorten the period of development, while Japan has expected it to reduce the chip area. Recently, Japan has come to use CAD for the same purpose as the United States" (David W. Hightower, U.S. Seiko Instruments Inc.).

Furthermore, this boom was strongly backed by the CAD system based on EWS (engineering workstation). Because of the appearance of this type of CAD system, designers on the user side became able to design gate arrays while conversing with computers, without paper, pencils, or breadboards. Thus, the number of designers allowed to take part in gate array design increased markedly.

At the same time, the CAD system market expanded so greatly that it became independent of semiconductor makers. Thus many ventures of CAD vendors flourished mainly in the United States. Because of the severe competition among these ventures, the EWS-based CAD system made great progress in a short period of time. The age of semicustom LSIs thus began to prevail from the 1980's, especially from 1985.

#### CMOS Gate Array Plays Leading Part

At first, the gate array appeared as a bipolar chip like TTL. In the first part of the 1980's, CMOS gate arrays were generally used.<sup>2</sup> They became larger and faster because of micronization, in addition to their inherent

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characteristic of low power consumption. In 1985, when the ASIC boom prevailed, CMOS gate arrays were the mainstream on the chip (Si) side.

In the latter half of the 1980's gate arrays of a channelless type, which made it possible to set up wiring channels freely, came to play the leading role.<sup>3</sup> Compared with the gate arrays of the conventional type (channel-fixed type), they make it possible to use the chip area effectively and are also suitable for the mixed loading of memories (especially SRAMs) as well as logical gates. Due to the appearance of the gate arrays of the CMOS channelless type, the charm of standard cells, especially the polycell type, was reduced by half.

In the late 1980's (around 1989), semicustom LSIs which had played a minor role, also came to be used widely.<sup>4</sup> These are linear arrays to realize analog circuits (Figure 5). Thus, the common knowledge that "semicustom LSIs are equal to digital LSIs" was no longer accepted. The analog LSIs that became associated with semicustom LSIs were not limited to linear arrays. An increasing number of semiconductor makers were keeping analog circuits in the cell libraries of standard cell LSIs as well.

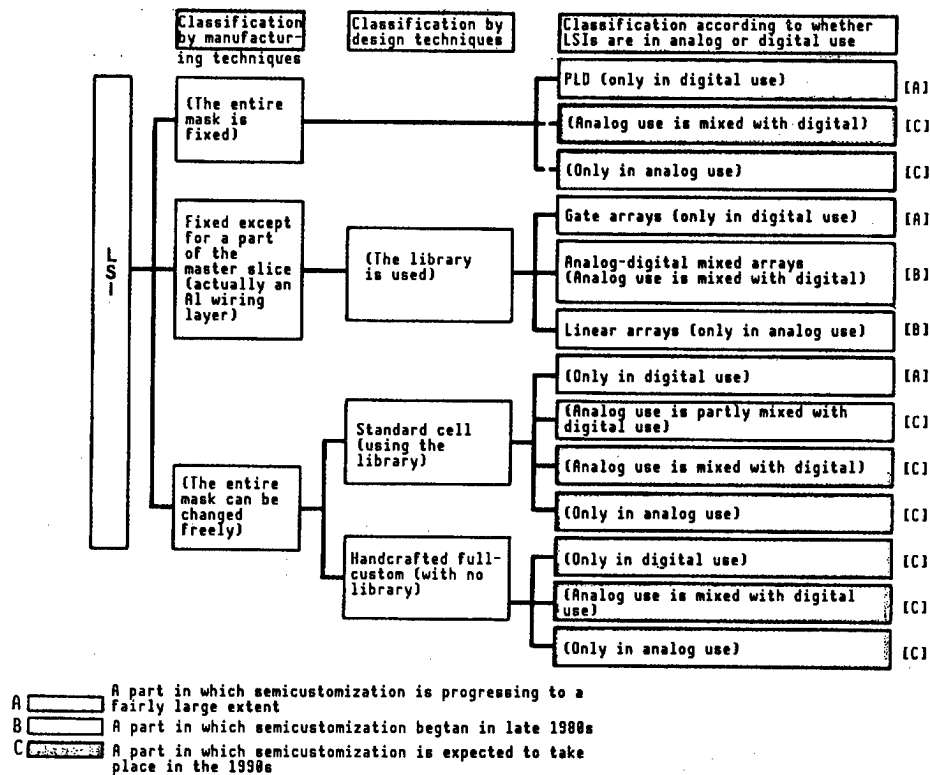


Figure 5. Analog Circuits Also Join Semicustom LSIs

In the late 1980's, analog LSIs were fully associated with semicustom LSIs. In the latter half of the 1990's, when silicon compilation is expected to be put into practical use, standard cells and handcrafted full-custom LSIs will be united and associated with semicustom LSIs. Many semiconductor makers think that analog program devices will also be put into commercial use during the 1990's.

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In the first half of the 1990's, too, CMOS channelless gate arrays will remain in the leading position. The largest number of stored gates currently obtainable on a chip is 200,000-250,000. Actually, 40-60 percent of them can be used as logical gates for users' designs. Fujitsu says that "In 1994, gate arrays each loaded with millions of gates will also appear."

In the latter half of the 1990's, building-block type standard cells are expected to become the mainstream. It will be possible to realize analog circuits, large-scale memories, etc., too, with comparative ease. These are difficult to achieve with CMOS channelless gate arrays. By around that time, large-scale logical blocks (megacells) are also expected to become complete in fairly large numbers. Silicon compilation will become a reality, and the age of building-block type standard cells will become unshakable.

### Algorithm Will Be Adopted for LSIs

In the case of semicustom LSIs, CAD tools, as well as chips, will become an important HOW to be shared by semiconductor makers (in some cases they are being shared by some makers exclusively dealing with CAD). Particularly, their

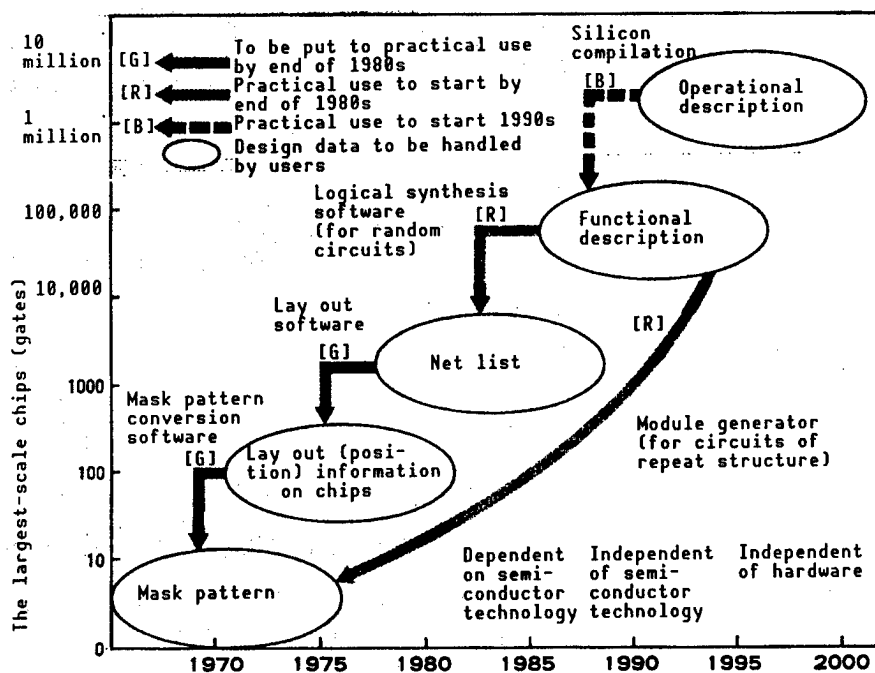


Figure 6. Development Toward Automatic Designs for Semicustom LSIs

Through the development of CAD tools, design data handled by users have been simplified. With logical synthesis software and module generators, users have been able to make LSI designs independently of semiconductor technology. If silicon compilation becomes practical, it will be possible to make LSI designs from operational descriptions (algorithm). From around 1985, the focus of computers using CAD tools shifted from large computers to EWSs, though this is not shown in this figure. (The illustration was based on reference No 7.)

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roles will become greater if chips become large and complex. As mentioned earlier, the EWS-based CAD system loaded with circuit diagram editors and logical simulators has freed designers on the user side from designing with paper, pencils, or breadboards. However, they had to design with cells designated by semiconductor makers and therefore were able to work independently. When they wanted summing circuits, for example, they had to use cells, while bearing in mind the design rule laid down by semiconductor technology.

At the end of the 1980's, it became possible to use logical synthesis software<sup>5</sup> and module generators<sup>6</sup> through EWSs (Figure 6). The first half of the 1990's was an age for these tools, and now designers can design chips independently of semiconductor technology. In both cases, they make designs by inputting the functional descriptions of required LSIs. The logical synthesis software is suitable for comparatively random circuits such as control circuits. The module generator displays its power in designing LSI structures of regular

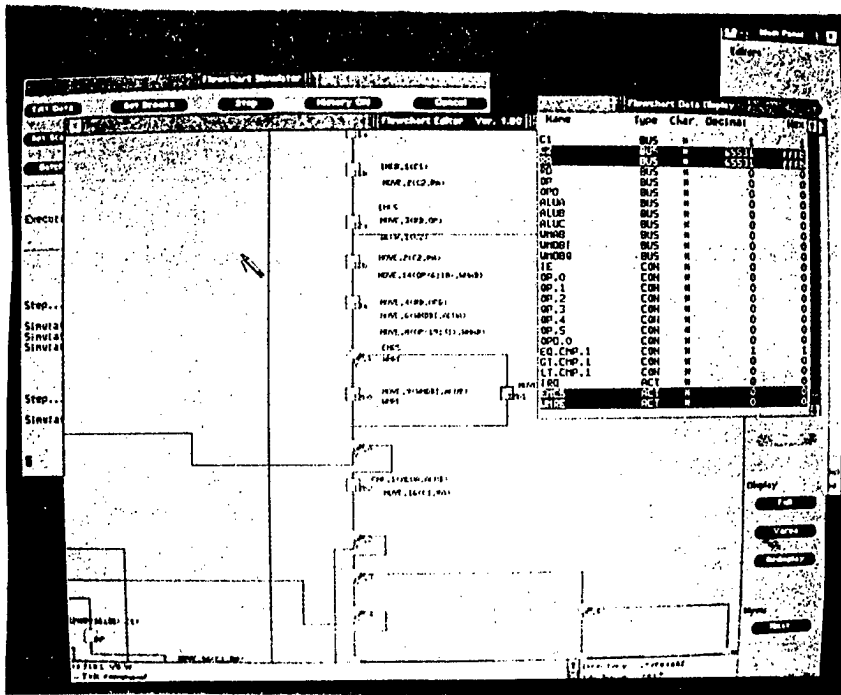


Figure 7. CAD Tool Capable of Input by a Flow Chart

This tool, though still restricted, is close in image to silicon compilation. Input is given by a flow chart and output by a net list for semicustom LSIs. A combination of this tool with layout CAD makes automatic designs possible for a flow chart and even for a mask pattern. Each step of the chart is described on such a level as summing instructions or move instructions. This tool, called KBSC, was developed jointly by Ricoh and ICC (International Chip Corp.) of the United States. After being used by Ricoh to design 20 product-level ICs, this tool was released also to semicustom LSI users outside the company. A certain parts maker finished designing a 5,000-gate gate array in a month using this tool. The chip was used in the printer region of a personal word processor that was put on the market in October 1989.

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repetition as seen in memories, ALUs, etc. Summing circuits, referred to as "circuits for addition," can be designed only by describing the functions of circuits (hardware).

In the latter half of the 1990's, silicon compilation will become a reality in forms that include the logical synthesis tool and the module generator. If users employ the silicon compilation, they will be able to make automatic designs in one step even for the mask pattern of a required LSI only by describing its operation (algorithm) (Figure 7). Thus, it will become unnecessary to have the awareness of hardware for summing circuits. Only the operation of "addition" has to be considered.

### Counterattack by Si Will Begin

Semicustom LSIs that have developed smoothly since the ASIC boom seem likely to reach their climax in the latter half of the 1990's because of the standard cells of the building-block type and the silicon compilation. If describing the algorithm alone is sufficient, an increasing number of set makers will be able to design the most advanced LSIs by themselves. Semiconductor makers could supply one custom LSI after another without requiring much time or labor for support. Therefore, it is likely that both makers and users will be pleased with their developments.

However, Si has called for a "wait" with regard to such developments. Some assumptions are required to bring this scenario to a happy conclusion, but these assumptions are not likely to be borne out (Figure 8). The gap between the assumptions and reality is not wide enough to change the direction of the story about semicustom LSIs in the 1990's. Even so, expectations must be revised because users and semiconductor makers who can take part in the happy story are unexpectedly few.

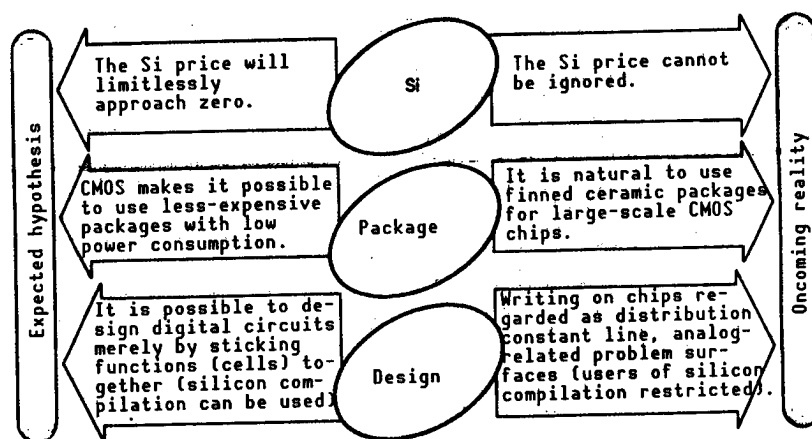


Figure 8. Gap Between Assumptions and Reality

The assumptions necessary for a happy ending have gotten out of touch with reality, and it has become necessary to revise the scenario.

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For example, the revised scenario will reveal the following development: it was assumed that the price of Si would limitlessly approach zero. In reality, however, the speed of a drop in the Si price per unit function slowed down (refer to Part 6). The Si price is not likely to become zero. Silicon compilation is basically a tool designed to "simplify designing even though Si involves waste." If Si does not become cheaper, the arena of its activity will be restricted.

In addition, the assumption that digital circuits could be designed by sticking cells together without regard for analogous conditions is also about to collapse. "From the age of CMOS gate arrays following an 0.8  $\mu\text{m}$  rule, it will become necessary to make designs regarding wiring as a distribution constant line" (Fujitsu, NEC, etc.). Users say that unless they take part even in layouts to some extent, they will be unable to elicit the performance of chips.

Silicon compilation subjected to various restrictions will become a tool for a limited number of professionals rather than a tool for everyone. When it is used properly, it can produce splendid results, but it is not serviceable at all for amateurs. If handled carelessly, it might become a dangerous tool. Thus, the number of users who can master the silicon compilation will become limited.

If the number of such users is limited, the competition among semiconductor makers will become severe. Various semiconductor manufacturing companies are currently supplying semicustom LSIs generally on the same level, but if the competition intensifies, some of them will drop out. Moreover, a huge quantity of facilities investment is necessary to provide microprocesses, and thus the number of semiconductor makers will be narrowed.

If their number decreases, the supply power of semicustom LSIs will drop. Then, users will be selected. For example, semicustom LSIs will be supplied only to users having WHAT that is attractive to semiconductor makers.

There is no guarantee that the revised scenario will unfold exactly as described here. However, it is certain that the story's happy ending will be tempered. At the time of the ASIC boom in 1985, the number of users capable of obtaining LSIs for their exclusive use appeared to increase in succession, thanks to semicustom LSIs. However, their number will be narrowed down again because of the counterattack by Si.

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### Part 5. Microprocessors Are Aimed at 1,000 MIPS Processing Performance and Integration of 100 Million Transistors

The improvement of the performance of 32-bit microprocessors will continue in the 1990's as well. In the first half of the 1990's, they will achieve 100 MIPS by such means as storing multiple pipelines. Furthermore, they may be able to achieve 1,000 MIPS in the latter half. Thus, they may possibly be used for computers of the mainframe class. A huge address space will become necessary to deal with data bases and multimedia. The 4G-byte address space does not suffice, and a foundation for the appearance of a 64-bit architecture will be created. If things go smoothly, the number of transistors that can be integrated in one chip may exceed 100 million before the 21st century.

The 32-bit microprocessors will reach a turning point in the 1990's. The method used in the 1980's will become unserviceable, and makers will be pressed to establish a new computer architecture and a new software technology.

Since the appearance of the 32-bit microprocessors in 1983, makers have been adopting the technology cultivated with the mainframe. Efforts have been made to improve their performance and functions after the model of hardware technologies for pipelines, caches, etc. However, these efforts will become fruitless.

There are many who say, "The age will end when the hardware for mainframes is targeted. The next target will be a supercomputer" (technicians for a Japanese microprocessor maker).

Some progress already has been made toward adopting such architectures as the superscalar, the superpipeline, or the VLIW (very long instruction word), for example, to increase performance by shortening the pipeline pitch or storing multiple pipelines, as in the case of supercomputers.<sup>1</sup> For the superscalar and the VLIW, multiple pipelines are to be put into one chip. In the case of superpipelines, the pipeline is to be fractionated. The performance is to be improved by shortening the executing time per step.

However, there are limits to such architectures as the superscalar and the VLIW. The number of processings capable of parallel execution through ordinary applications is said to be two or three. Even if the number of pipelines is increased at random, performance will not improve. The limit will appear in the middle of the 1990's, when it will become possible to store about four pipelines. Thus, the search for an architecture exceeding the superscalar and the VLIW will begin.

#### Performance Will Exceed 100 MIPS in the First Half of the 1990's

In the first half of the 1990's, the performance of 32-bit CMOS microprocessors will continue to improve through introducing the superscalar and VLIW architectures. In the early part of the 1990's, the processing power will exceed 100 MIPS. Through some breakthrough or other, makers will likely come to aim at achieving 1,000 MIPS toward the end of the 1990's.

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The value of 100 MIPS is equal to that of the current top-level mainframe machine. When the machine improvement in the performance of the mainframe is estimated, "their MIPS value will rank with that of the top-level mainframe machine (single processor) around 1995" (Intel Corp.).

If so, the scope in which 32-bit microprocessors are applicable will no longer be limited to personal computers or workstations. They are already being mounted in minicomputers and office computers, and this trend will become increasingly strong.<sup>2</sup> There is even the possibility that they will advance into computers on the mainframe level (Figures 1 and 2).

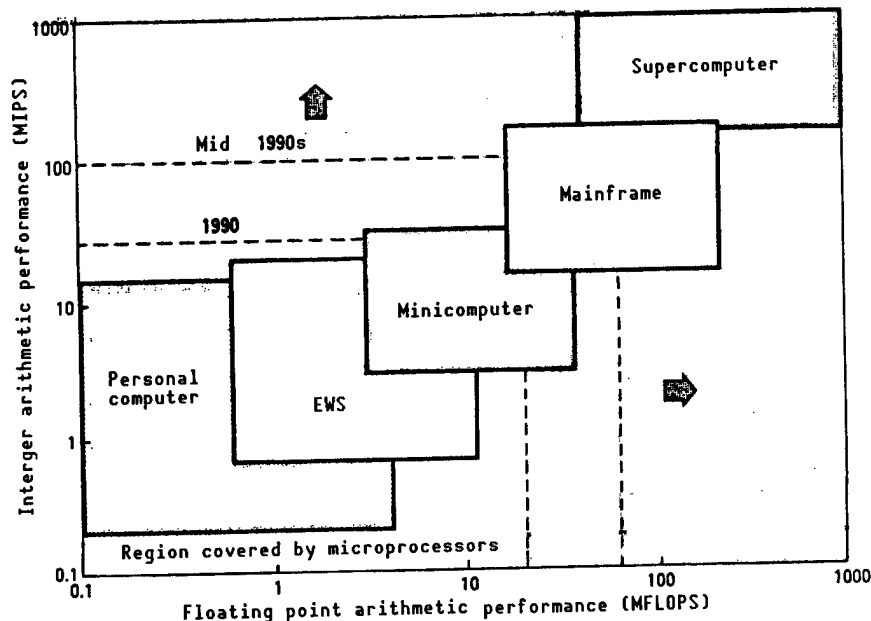


Figure 1. Scope of 32-Bit Microprocessor Applications Is Expanding

The improvement in the performance of 32-bit microprocessors is remarkable. With this improvement, the scope of their applications is continuing to expand. Minicomputers, office computers, etc., have also begun to use 32-bit microprocessors on the market. This trend will continue in the 1990's as well. The scope of their applications may expand to computers of the mainframe class.

The scope of applications will also expand. The 32-bit microprocessors will be used for data bases requiring high processing power and for the processing of multimedia. Both need large address spaces. The 4G-byte address space supported by 32-bit microprocessors will become insufficient, and this will urge the development of a microprocessor with a 64-bit architecture.

### Memory Capacity "Three Times the MIPS Value" Will Be Necessary

A rise in the ability of a microprocessor will be useless if the performance of an entire system does not improve. It is necessary to make memory system and system bus designs matching the processing ability of microprocessors.

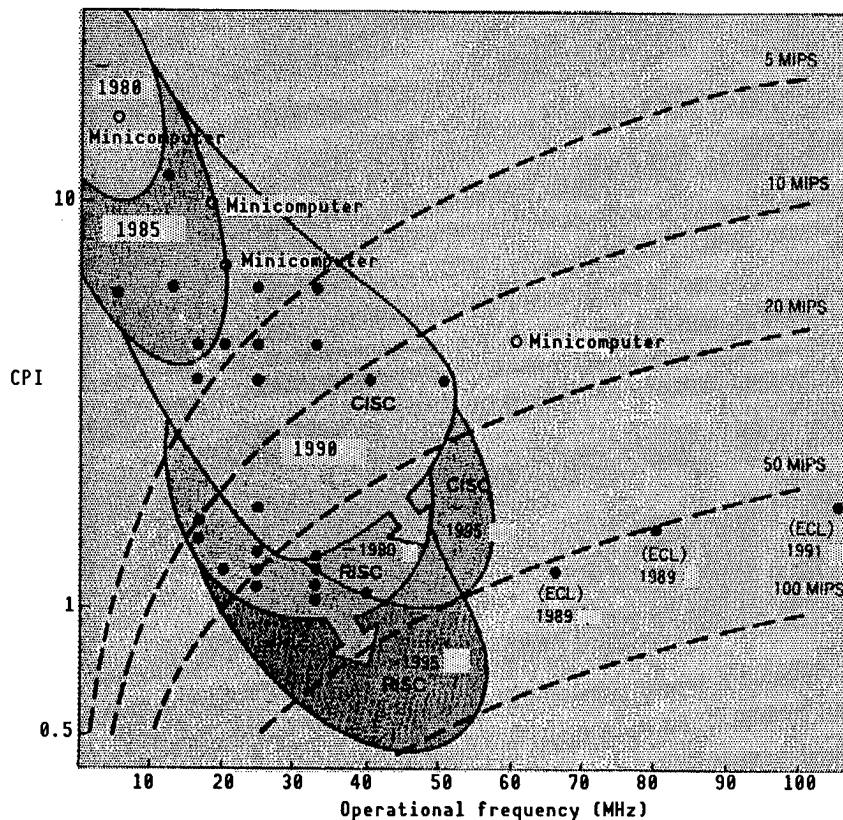


Figure 2. 32-Bit Microprocessor That Will Greet 100-MIPS Age

The CPI (number of clocks needed to execute one instruction) of 32-bit microprocessors is becoming smaller and smaller. In the 1990's, the CPI will become less than 1.0 through the inclusion of the parallel processing mechanism. Coupled with the improvement of operational frequency, the MIPS value is rising steadily. It will exceed 100 MIPS by the middle of the 1990's.

For example, the capacities of the main memory and the cache must be increased in accordance with the performance of a microprocessor. When the capacity of the main memory is small, access to external memories such as the magnetic disk occurs frequently. This brings about a bottleneck. The higher the processing power of a microprocessor, the higher will be the rate of access to external memories to processing hours. Therefore, the system performance will not rise as much as expected.

How, then should the capacity of the main memory be determined? One criterion may be that "the capacity of the main memory should be three times the MIPS value" (designer for a Japanese workstation maker), though this varies with the desired applications. A system loaded with a 100-MIPS microprocessor needs a 300M-byte main memory.

The cache is also important, because the pipeline will become out of order if access to the cache memory cannot be effected with zero wait. However, an improvement of the operational frequency of microprocessors causes the cycle

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hours of the bus to become shorter and shorter. Thus, the zero wait access to the cache memory has become difficult. Some are saying that "such matters as the protocol and timing of the bus must be reconsidered" (Motorola Inc.) in order to facilitate cache designs.

### ASIC Development Will Become Indispensable

When the 32-bit microprocessors in the 1990's are considered, the move to produce chips for exclusive use also cannot be overlooked. Behind this move is an increase in the number of transistors that can be integrated into one chip.

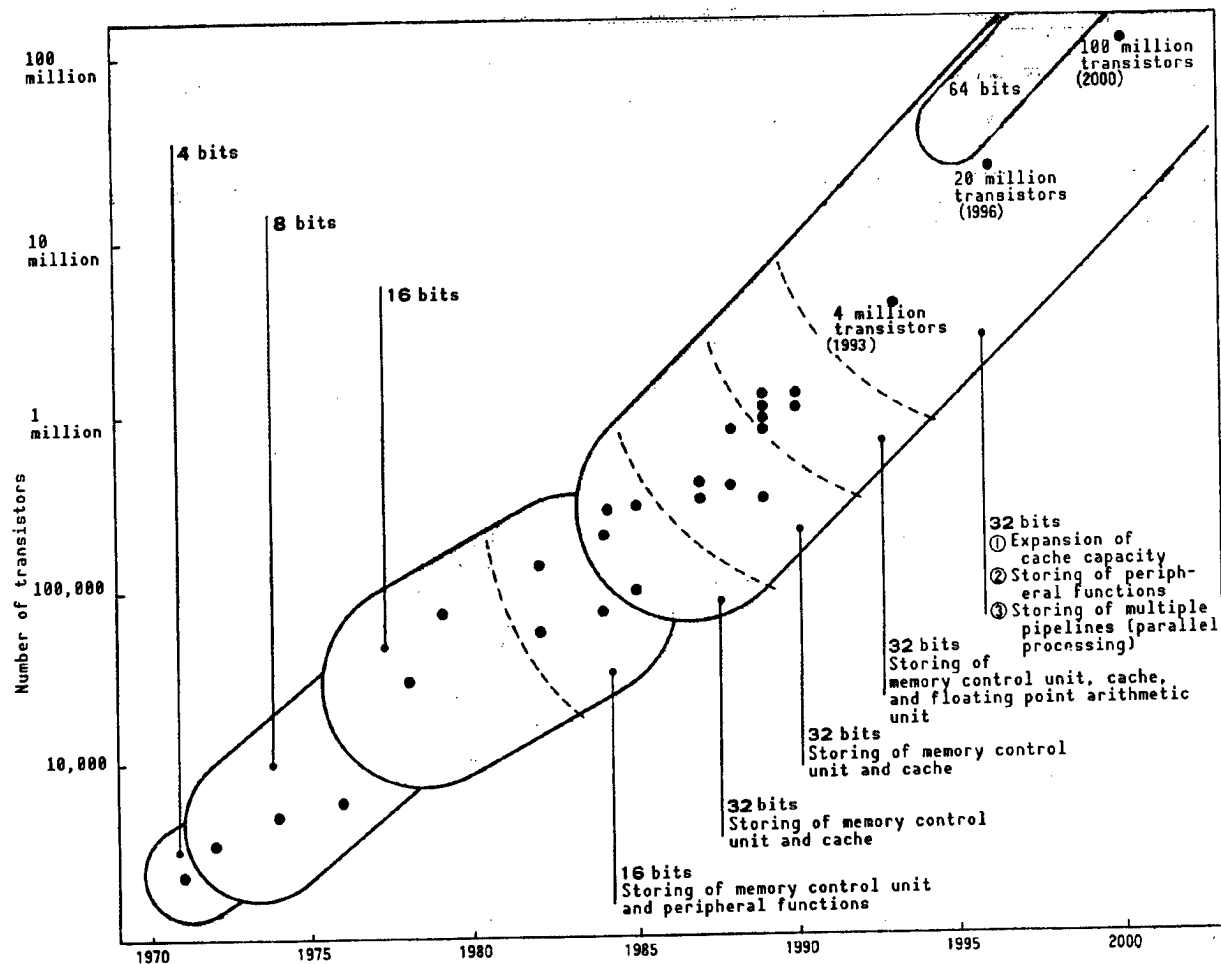


Figure 3. ULSI Age Approaching

The number of transistors to be integrated into one chip in a 32-bit microprocessor is continuing to increase 1.4-fold every year. In 1989, a chip consisting of 1.2 million transistors appeared. Thus, it has become possible to store most general-purpose functions, such as memory control units, floating point arithmetic units, and caches. There are also some who predict that the number of these transistors will exceed 10 million around 1995. An ASIC-like development to incorporate functions desired by users will become essential. The finish of CAD tools holds the key to success.

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If 1.2 million transistors can be integrated into one chip, it will be possible to store most general-purpose functions including memory control units, caches, and floating point arithmetic units. In the mid-1990's, it will become possible to integrate 5 million transistors (Figure 3). If things go smoothly, "integration of 100 million transistors will be possible at the end of the 1990's" (Intel Corp.).

Even when such general-purpose functions are stored, silicon will still have more space in reserve. It can probably be said that an ASIC-like development toward putting functions desired by users into an empty space is a natural course of development.

If such is the case, perfection of CAD tools will become more important than ever.<sup>2</sup> If one chip is to be stored with 5 million transistors, it will be impossible to make designs through handiwork. It will become indispensable to use a method for chip designs by registering LSI in building-block libraries and combining these libraries. It can be said that the finish of CAD tools including the libraries holds the key to ASIC development.

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### Part 6. There Are No Limits To Expanding the Scale of Integration, But Micronization Will Become Increasingly Difficult

There is no theoretical limit to the scale of LSI integration. However, in practice, a limit is being reached: the fall in per-function price will slow down. Even so, efforts for micronization are not discontinued. The age of silicon or the age of transistors will continue during this century.

When will the limit of silicon ICs come? This is a question that has been repeated since the appearance of ICs. There are always two answers to this question: 1) they will have no limit, and 2) they have reached their limit at present.

As long as the chip area can be expanded, there is effectively no limit to the scale of integration. If conditions existed in which price were no object and unlimited supplies of funds or labor were available, it would be possible to achieve almost anything, and therefore no limit would exist.

If LSIs are to be manufactured under actual conditions and restrictions, they are always to be manufactured at the very limit. In this sense, "they have their limit at present."

One response might be that "there is probably a limit due to physical conditions." However, if it is possible to use silicon produced in an ideal form and to control the distribution of impurities just as desired, and if there is no warp at all in processing size, the limit will be a matter of the distant future. Moreover, if LSI can be cooled to the temperature of liquid nitrogen, for example, without regard to their being operated at room temperature, it will be still longer before the limit is reached. If superconduction wiring can be used freely, the limit will be still more remote.

There are also cases where the constant of a physical property, which determines the physical limits, undergoes a change due to progress in manufacturing technology. "Our technologies have not reached a state where we can discuss the strict theory of limits. There is an instance in which the constant of a physical property varies with each measurer by about one digit" (Tadahiro Ohmi, professor of the electronic engineering department, engineering faculty, Tohoku University). If clean materials are created with the progress of manufacturing technology, the constants of physical properties will change, and this will result in the limits being regarded as remote again.

In the final analysis, the limits will always be represented by a point most currently reached through constant efforts to overcome present restrictions. Therefore, the limits are "something usual."

The manufacturing side says that "Linear extrapolation is no longer possible; we are about to reach the limit." But the user side is optimistic, making this rebuttal: "Makers always make such an assertion, but the extrapolation line has never bent. They are like the boy who cried wolf." This is also a familiar scene.

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### There Are Signs of Limits

Looking over the 1990's, however, it seems unlikely that makers can be accused of crying wolf. It is difficult to give any clear physical explanation about this, but the atmosphere of the semiconductor community is gradually revealing that the future is not always an extension of the past.

With regard to memories, for example, the bi-rule<sup>1</sup> that the per-chip price doubles each time one generation is replaced by another is gaining strength. Also, users may have come to recognize reluctantly that it is impossible to design for systems on the premise that "silicon will be obtainable for nothing some time in the future." This atmosphere was created in the process of overcoming the depression of 1985, and it has taken concrete shape in the late 1980's.

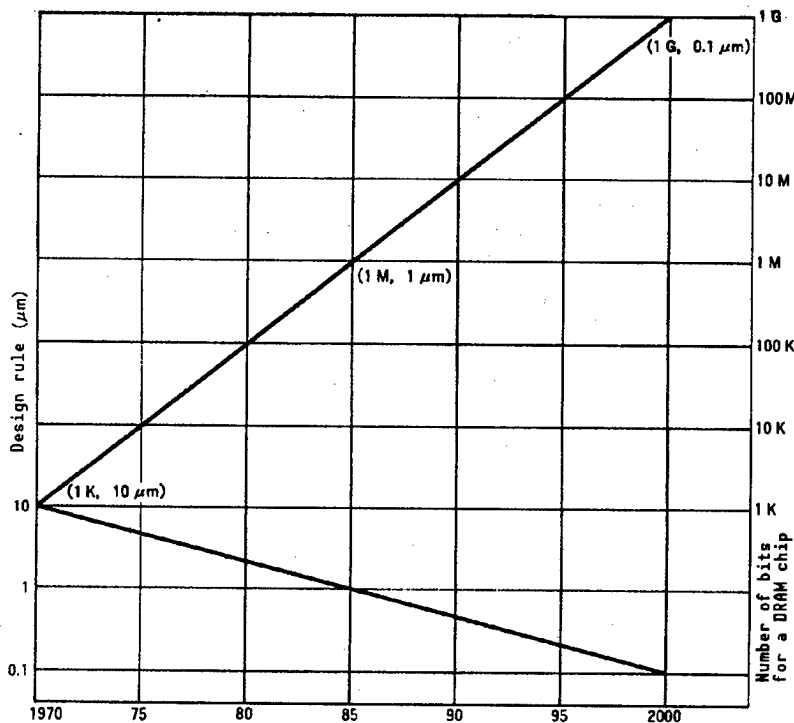


Figure 1. Changes in Micronization and Scale Expansion

The design rule (minimum processing size) has been reduced to one-tenth in 15 years. During this period, the number of memory bits on one chip has increased 1,000-fold. In 1970, a 1K-bit DRAM was produced with the 10-μm rule, and in 1985 the 10 μm was reduced to 1 μm and the 1K increased to 1M. If the same pace continues, these will become 0.1 μm and 1G in 2000.

The year 1985 is symbolized by 1 μm and 1M bits. That year the design rule for trial manufacture was 1 μm, and the 1M-bit MOS dynamic RAM was developed. As 1K DRAMs were produced by the 10 μm design rule in 1970, the size has been reduced to one-tenth and the memory capacity has increased 1,000-fold.

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When this trend is extrapolated, the design rule will become  $0.1\ \mu\text{m}$  and the capacity of a DRAM chip will reach 1G bits (Figure 1).

### Limits to Manufacturing and to Markets Are Complementary

Funds are among the restrictions swaying the limits. With the progress in micronization and the expansion of the integration scale, the cost of manufacturing equipment becomes higher and the expenses for ensuring clean investments become heavier. The paces of these increases are accelerated as the processing size becomes smaller. The manufacturing side says that "The amount of investments becomes too large, and there is no guarantee for their recovery."

The amount of recoverable information varies with the market size. It is possible to make an investment if there is the guarantee that manufactured products will sell. In other words, the growth of a market sways the limit.

The growth of the semiconductor market is determined by the market for equipment and systems that are used through the incorporation of semiconductors. The growth of the equipment market is influenced by the entire consumption market or gross national product (GNP).

As long as the market for electronic machinery and equipment is small, the scale of the economy as a whole need not be considered. However, production in the Japanese electronic industry, for example, has exceeded ¥20 trillion, approaching 10 percent of the GNP. Those who are connected with the market for machinery and equipment cannot fail to note the ceiling of the GNP. Similarly, those who are connected with the semiconductor market will inevitably become aware of the market ceiling for machinery and equipment. It was probably in 1985 that such a stage was reached. This is also proof that the semiconductor industry has become large.

When the market became aware of the ceiling, the manufacturing technology became aware of the barrier to submicron LSIs. The manufacturing side began to try to recover facilities investments through price increases rather than through quantitative expansion. In other words, the limits appear in terms of a rise in the price of semiconductor products (slowdown of a fall in per-function price), for the time being. Users also show signs of recognizing it, though reluctantly. However, the growth in the number of semiconductors used will slow down, as a matter of course. The conversion from quantity to quality symbolizes the "limit." In the background, there is the final consumption market oriented toward added values. In the consumption market, the age of price reduction and mass production has ended. Semiconductors also are not unaffected by this.

### Micronization Must Be Promoted While Achieving High Performance and High Reliability

For more than 10 years, the guiding principle for micronization has been the so-called proportional reduction (scaling). When the size of a device is to be reduced to  $1/S$  in the basic structure of the MOSFET given in Figure 2, other

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parameters are fixed in the way given in Table 1. The gate delay is shortened to  $1/S$  and power consumption is reduced to  $1/S$  (the power consumption per unit area is not changed). These are all favorable. However, if they are the only results that can be obtained, various disadvantages will arise. It can be said that overcoming these disadvantages is a task for micronization designed to break through the limits.

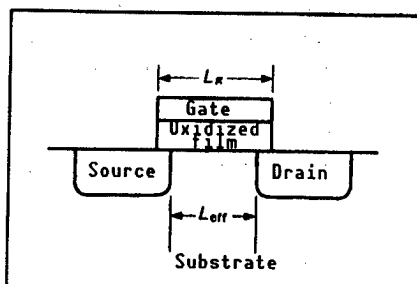


Figure 1. Basic Structure of MOSFET

In many cases the minimum processing size (design rule) is represented by gate length  $L_g$  or effective channel length  $L_{eff}$ .

Table 1. Proportional Reduction Rule

(Showing how other parameters will turn out when the size of a device is reduced to  $1/S$ .)

Parameter	Rate of reduction
Device size	$1/S$
Density of substrate impurity $N_A$	$S$
Gate capacity $C$	$1/S$
Voltage $V$	$1/S$
Electric current $I$	$1/S$
Gate delay $CV/I$	$1/S$
Power consumption $VI$	$1/S^2$
Product of power and delay time	$1/S^3$

Only micronizing individual transistors will not bring work to an end. Higher performance and higher reliability must be simultaneously achieved for them as LSIs (Figure 3). For example, no matter how microscopically a transistor may be produced, it will be meaningless if signals are buried in noise.

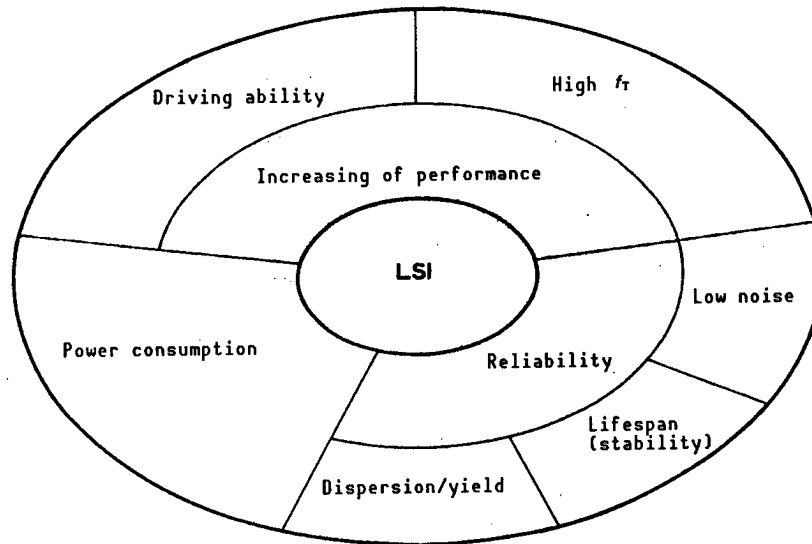


Figure 3. Relationship of Items To Be Achieved With the Micronization of LSIs  
(By Ohmi and Miyawaki)

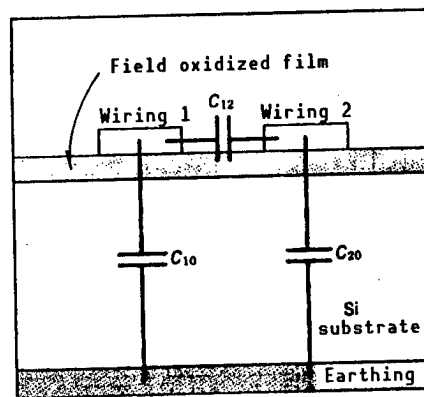


Figure 4. Typical Illustration of Two Wirings

In this sense, the crosstalk between wirings cannot be dealt with only through the proportional reduction mentioned earlier (Figure 4). If micronization proceeds, neighboring wirings will come close to each other, as a matter of course. The mutual capacity between wirings will increase and the crosstalk will gain strength. From the viewpoints of operational speed and power consumption, it is naturally desirable to reduce the resistance of wiring. If the wiring metal is thickened for this purpose, the coupling capacity between two opposite wirings will increase. Such trade-offs are innumerable, and compromises among them are necessary.

#### There Are No Materials Surpassing Silicon

The factors of limits arising with the micronization of elements are summed up in Table 2. Besides these, limits arise from manufacturing techniques. Lithography, in particular, is a key to microscopic processing, and it is becoming increasingly difficult. How far it is possible to produce LSIs through mask

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Table 2. Factors of Limits Arising With Micronization

	Items	Causes	Phenomena
Physical limits	Power-source voltage	Hot carrier impact ionization Breakdown voltage of oxidized films of gates Thermal noise	Shortening of lifespan Unsatisfactory operation " "
	Semiconductor band structure	Materials are limited to Si and SiO <sub>2</sub>	Ideal scaling is impossible
	Tunnel phenomena	Band-band of Si Tunneling of SiO <sub>2</sub>	Unsatisfactory operation due to junction leak, etc.
Limits in the actual aspect	Operational temperature	Most MOS LSIs operated at room temperature Operation at low temperature brings about a cost increase	Ideal scaling is impossible
	Parasitic effect	Source-drain parasitic resistance Contact resistance strong Wiring resistance; parasitic capacity	$g_m$ deteriorates Propagation delay deteriorates
	Noise	$\alpha$ -ray soft error Thermal noise Interwiring crosstalk	Malfunction
	Power consumption	Increase in number of elements and in length of wiring	Increased power consumption
	Fluctuation in device property	Fluctuation in manufacturing process	Drop in yield, performance
	Cost	Increase in manufacturing cost	
	Circuit design	Cost for circuit design; design duration	

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transcription by means of ultraviolet rays has always been, and remains, a topic of discussion.

Currently, the so-called stepper is the mainstay exposure system. An expanded mask (reticle) is to be projected while it is reduced by means of an optical system, and exposure for each chip is to be repeated. When the limits of this stepper and also of ultraviolet rays will be reached is a key question in the issue of manufacturing techniques.

Ultraviolet technology has survived through repeated improvements, with its limits pointed out for some time. Some other systems have been suggested for adoption, but it is impossible at present to evaluate their applications to mass production. Ultraviolet rays will continue to be used tenaciously for the foreseeable future.

Some of the factors mentioned in Table 2 are due to the inherent nature of silicon. Is there any material that can replace silicon? What will a post-silicon be?

This is another question that has been asked repeatedly. As far as LSIs are concerned, however, it should be considered that there will be no material surpassing silicon. "There is no material that can replace silicon. the reliability of silicon devices is great. Look at the 4M DRAM, in which 10 million elements are in operation. The 10 million is equal to the population of Tokyo. Almost all these elements are functioning accurately. No other materials can function like this. The post-silicon is silicon" (Kenji Natori, chief researcher of Toshiba ULSI Research Laboratory).

Semiconductive materials other than silicon are used even at present on a supplementary basis. Light-emitting devices are compound semiconductive products such as GaAs and GaP. GaAs transistors and ICs are used for micro-waves as well. However, these are supplementary to silicon, which is not to be replaced by them. The age of silicon will continue.

### Proportional Reduction Seems Applicable to the Extent of $0.3 \mu\text{m}$

The rule of proportional reduction is even now applicable as a guiding principle. It is said that proportional reduction will progress to the extent of  $0.3 \mu\text{m}$ ,<sup>3</sup> provided that various mechanisms are devised for device structure and so forth without applying Table 2 in a simple way.

The diversion of various parameters will become a serious problem with the increase in the number of integrated elements. Ohmi emphasizes the importance of restraining the diversion as much as possible, saying that the worst value determines the real ability of a system. Ohmi cites as an example the effect of impurity concentration upon threshold.

According to the rule of proportional reduction in Table 1, the impurity concentration will rise, which usually causes an increase in diversion as well. This brings about an increase in the diversion of threshold, too, and the threat of malfunction becomes strong. Thus, efforts are required not only

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for micronization but also for manufacturing with exactly the same value as is aimed at.

### Micronization Will Continue

When it becomes difficult to proceed with micronization in manufacturing technology and device structure, some contrivances for circuits or architecture may come into play. This is a new and old problem. Introduction of many-valued logic and functional devices becomes a subject for study. To date, the digital technology with two values has always been dominant. Various functional devices have been proposed one after another, but they have always been rejected, and simple transistors are currently used continuously. How will this situation turn out? If the difficulty of micronization becomes too great, a methodological contrivance may be the next turn.

Even so, many researchers believe that this will not make micronization unnecessary. "If micronization is not pursued, the semiconductor industry will cease to grow. In the field of semiconductors, it can be achieved if tackled with belief. Systematization or creation of intelligent devices is important, but this is a different technology" (Natori). "We will not discontinue micronization. If we think lightly of scaling, we will cry over scaling. We must do all we can, pursuing the utmost limits" (Eiji Takeda, chief researcher of Hitachi Central Research Laboratory).

As to how far micronization will continue,  $0.1\text{ }\mu\text{m}$  is regarded as an abstract limit, for the time being. This is an appropriate value. It will be called into question around 2000, and this is also appropriate timing.

It is said that individual transistors can operate at room temperature even when the minimum design size is  $0.1\text{ }\mu\text{m}$ .<sup>4</sup> However, when it comes to the problem of their having a scale befitting the  $0.1\text{ }\mu\text{m}$  rule as an LSI and achieving sufficient performance and reliability, many difficulties are involved, including manufacturing techniques.

There is also the problem of size in the case of electrons' beginning to reveal their nature as waves in terms of quantum dynamics. This threatens to bring about a malfunction of circuits. At the same time, new devices using the quantum effect in a positive way may become possible. Quantum devices are already attaining popularity in the realm of basic research.

Even so, the application of such devices will be in the 21st century, even if it is promoted very smoothly. During the 20th century, the age of silicon LSIs and transistors will continue.

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